Q190

Rev : 1.0

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NOTE:
Design by
471984_471984_Chief_River DG_1.5.pdf
474146_474146_PPT_EDS_Rev1_8.pdf
473716_473716_Ivy_Bridge_EDS_Mobile[1].pdf

REVISION HISTORY:

Rev	Date	Notes
V0.1	12/03/20	
V0.2	12/07/03	

[redacted] Bitland Information Technology Co.,Ltd

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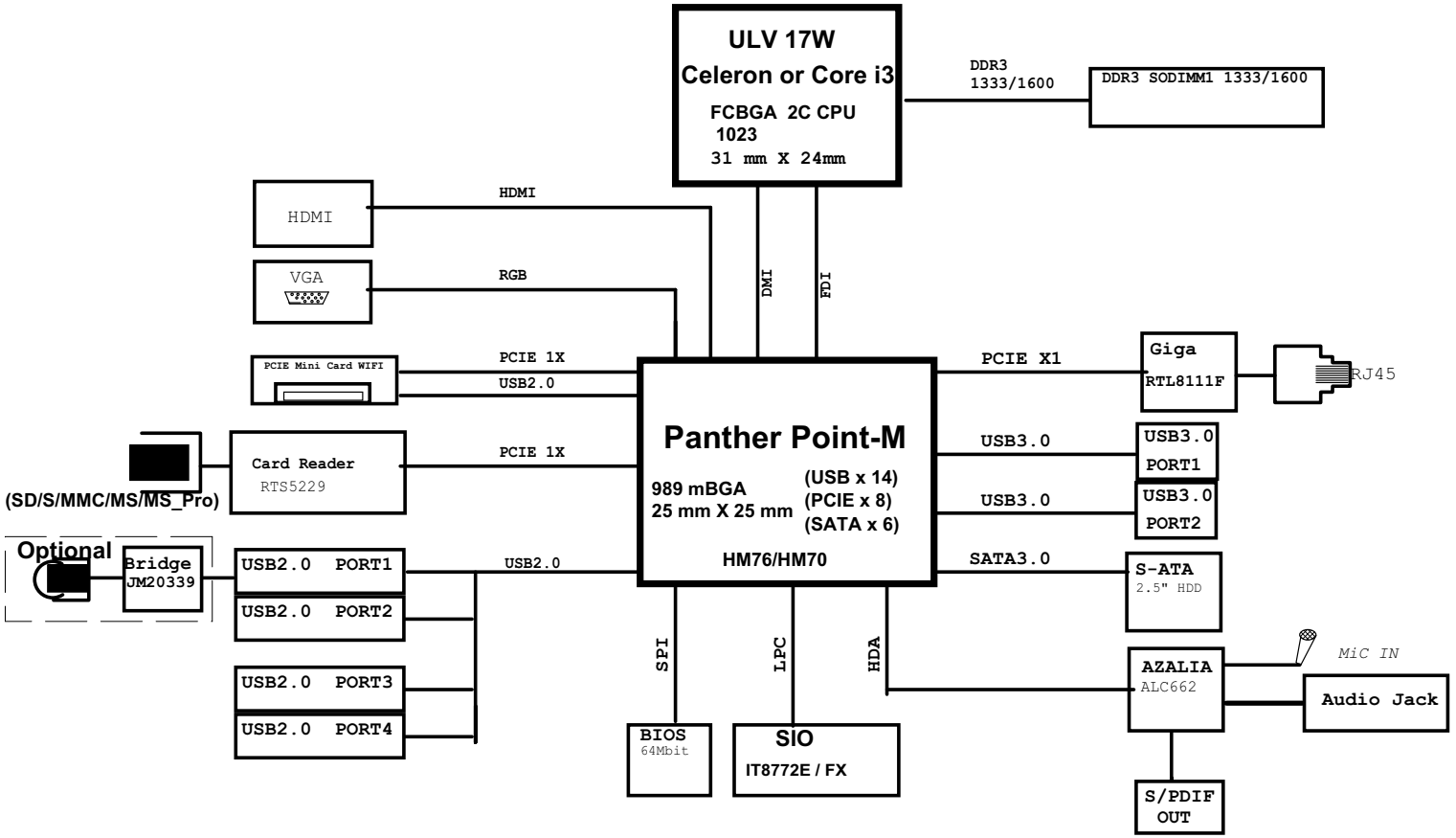
SYSTEM BLOCK



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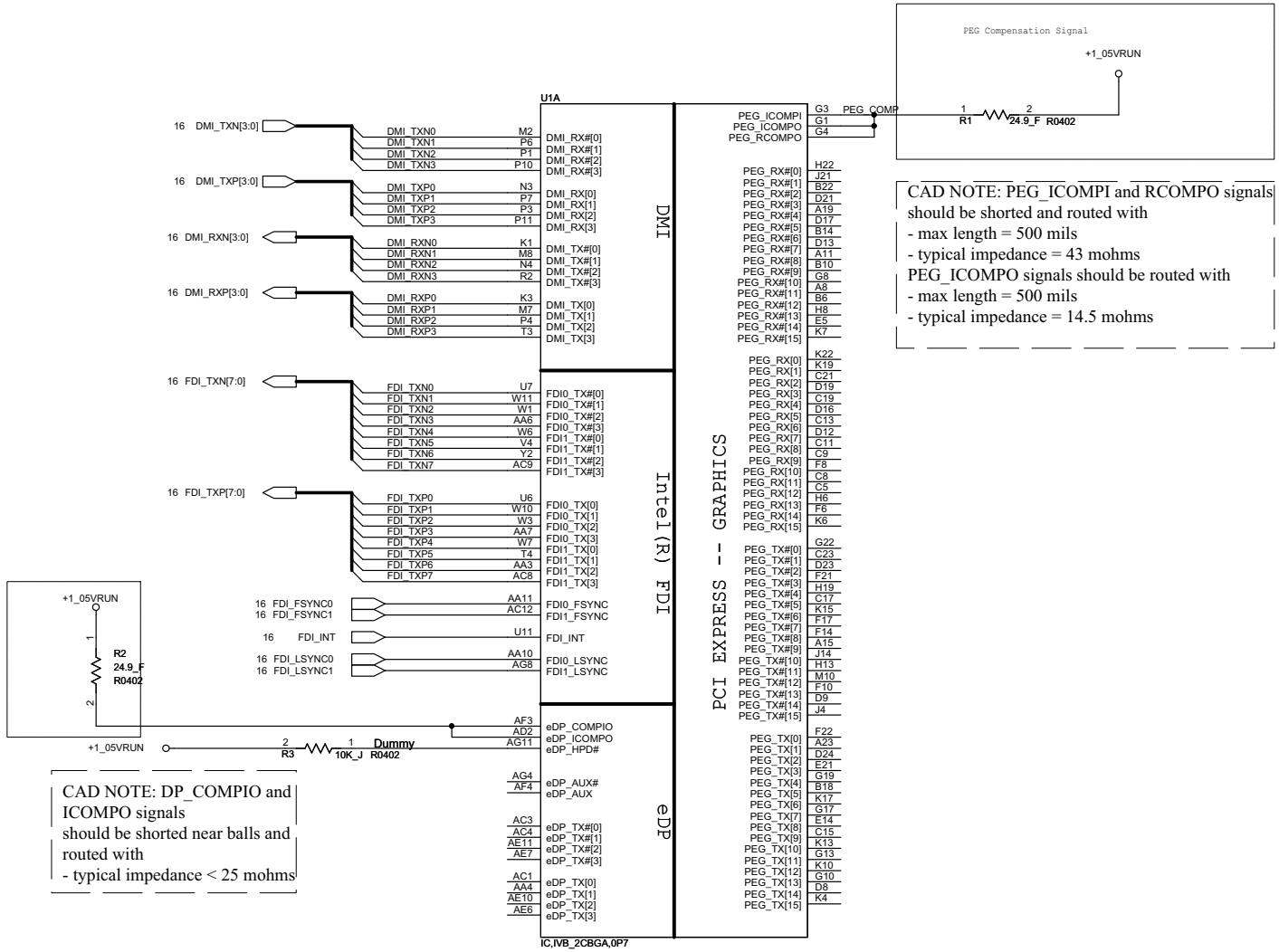
SANDYBRIDGE 2C BGA PROCESSOR (DMI,DP,PEG,FDI)



CAD NOTE: PEG_ICOMPI and RCOMPO signals should be shorted and routed with
- max length = 500 mils
- typical impedance = 43 mohms
PEG_ICOMPO signals should be routed with
- max length = 500 mils
- typical impedance = 14.5 mohms

CAD NOTE: DP_COMPIO and ICOMPO signals
should be shorted near balls and routed with
- typical impedance < 25 mohms

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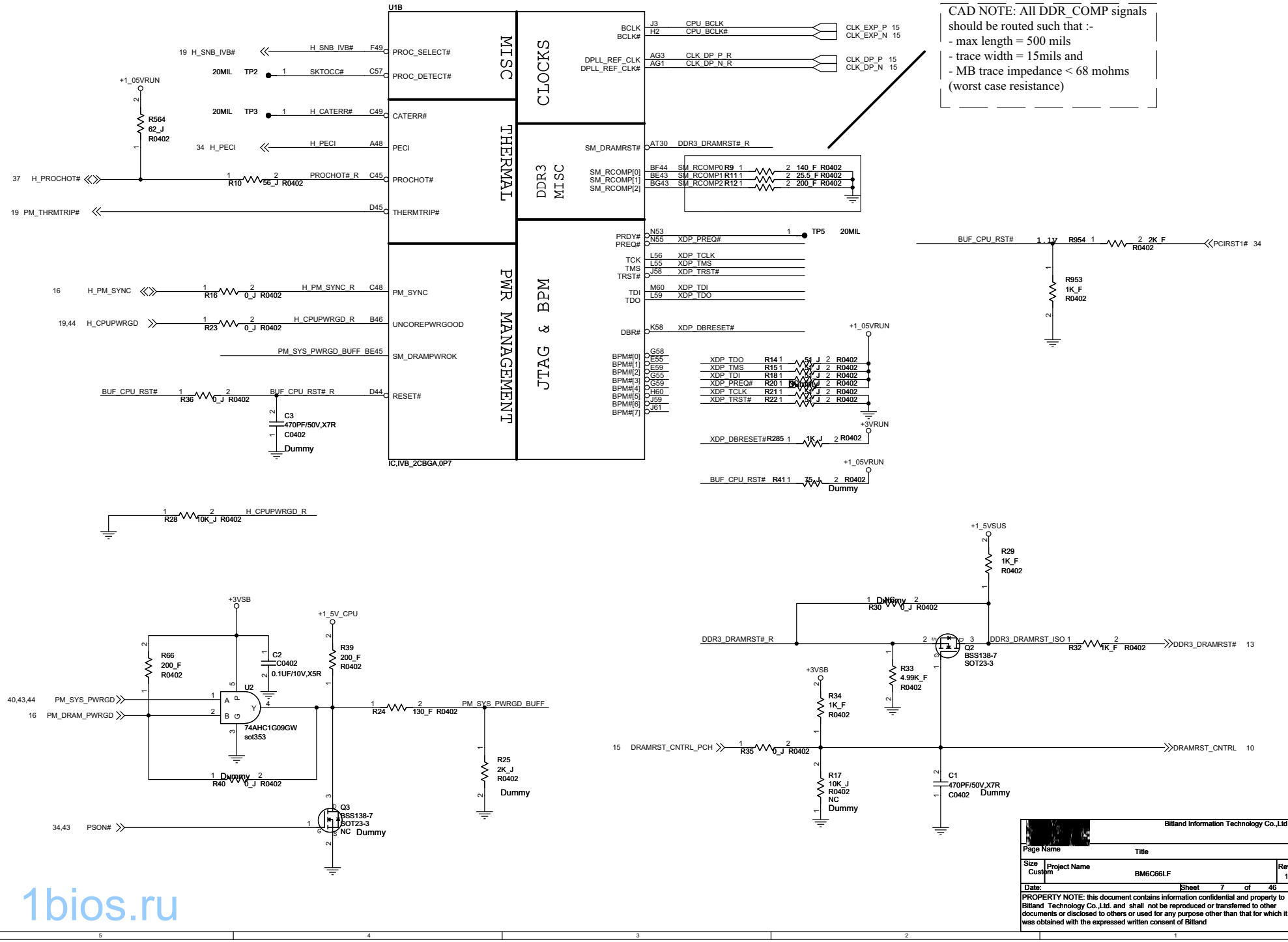
U1B
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
IC,IVB_2CBGA,0P7
CAD NOTE: All DDR_COMP signals should be routed such that :-
- max length = 500 mils
- trace width = 15mils and
- MB trace impedance < 68 mohms
(worst case resistance)
PROC_SELECT#
PROC_DETECT#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#
BCLK
BCLK#
DPLL_REF_CLK
DPLL_REF_CLK#
SM_DRAMRST#
SM_RCOMP[0]
SM_RCOMP[1]
SM_RCOMP[2]
PRDY#
PREQ#
TCK
TMS
TRST#
TDI
TDO
DBR#
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
BPM#[4]
BPM#[5]
BPM#[6]
BPM#[7]
H_SNB_IVB#
SKTOCC#
H_CATERR#
H_PECI
PROCHOT# R
H_PROCHOT#
PM_THRMTRIP#
H_PM_SYNC
H_PM_SYNC_R
H_CPUPWRGD
H_CPUPWRGD_R
PM_SYS_PWRGD_BUFF
BUF_CPU_RST#
BUF_CPU_RST# R
CPU_BCLK
CPU_BCLK#
CLK_DP_P_R
CLK_DP_N_R
DDR3_DRAMRST# R
XDP_PREQ
XDP_TCLK
XDP_TMS
XDP_TDI
XDP_TRST#
XDP_DBRESET#
XDP_TDO
PCIRST1#
DDR3_DRAMRST_ISO
DDR3_DRAMRST#
DRAMRST_CNTRL_PCH
DRAMRST_CNTRL
PM_SYS_PWRGD
PM_DRAM_PWRGD
PSON#
+1_05VRUN
+3VRUN
+1_5V_CPU
+1_5VSUS
+3VSB
74AHC1G09GW
sot353
BSS138-7
SOT23-3
Dummy
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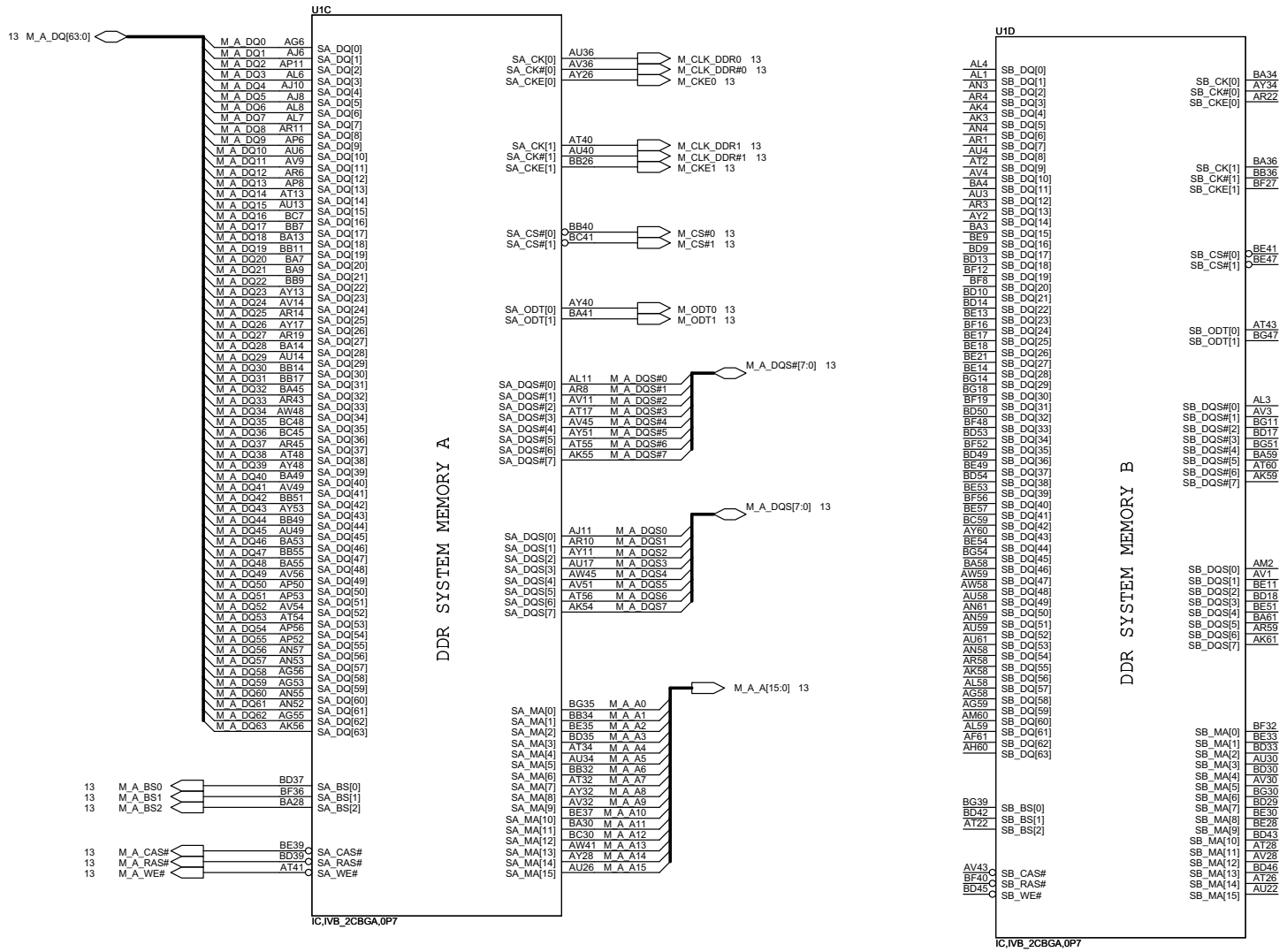

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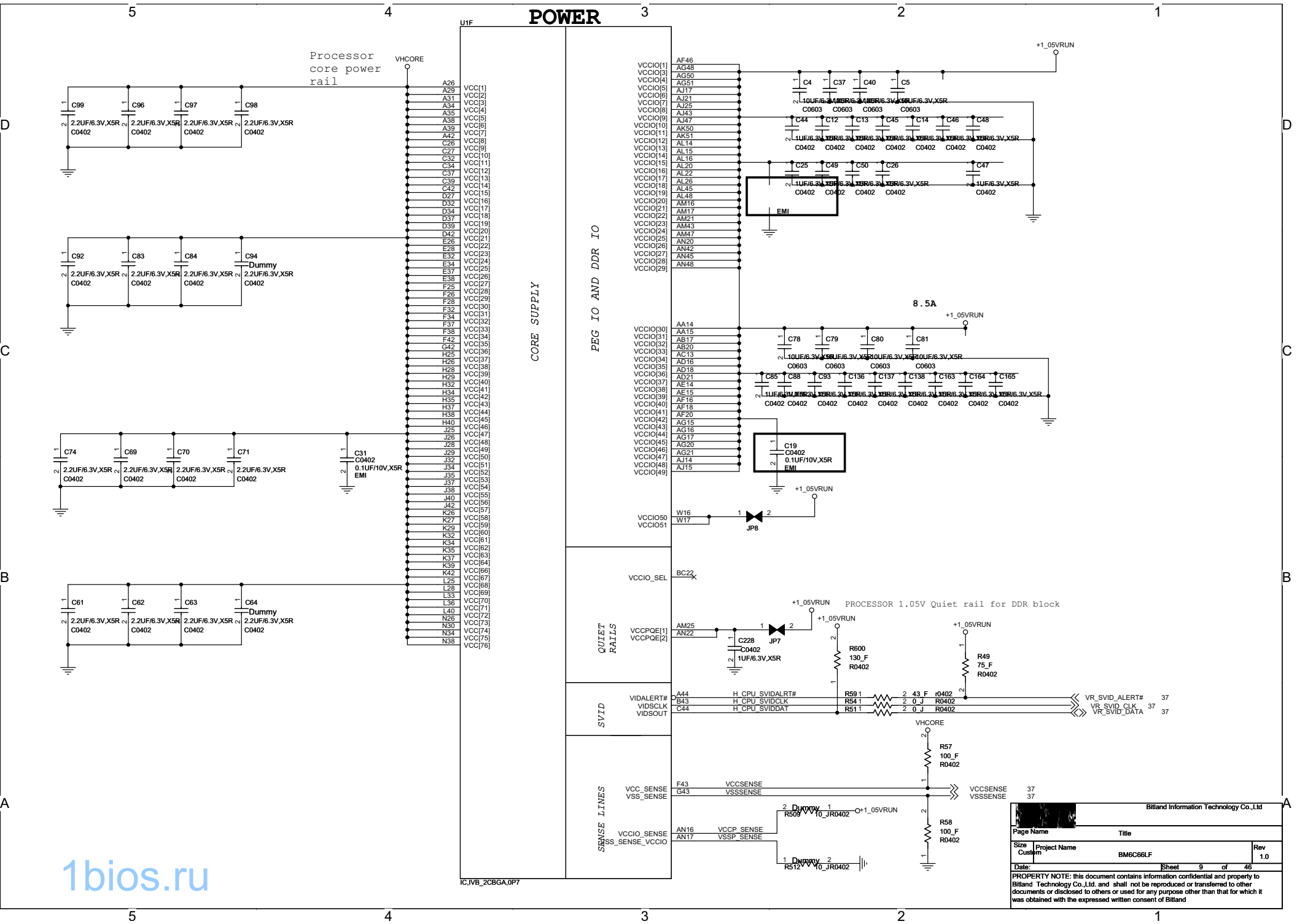
POWER



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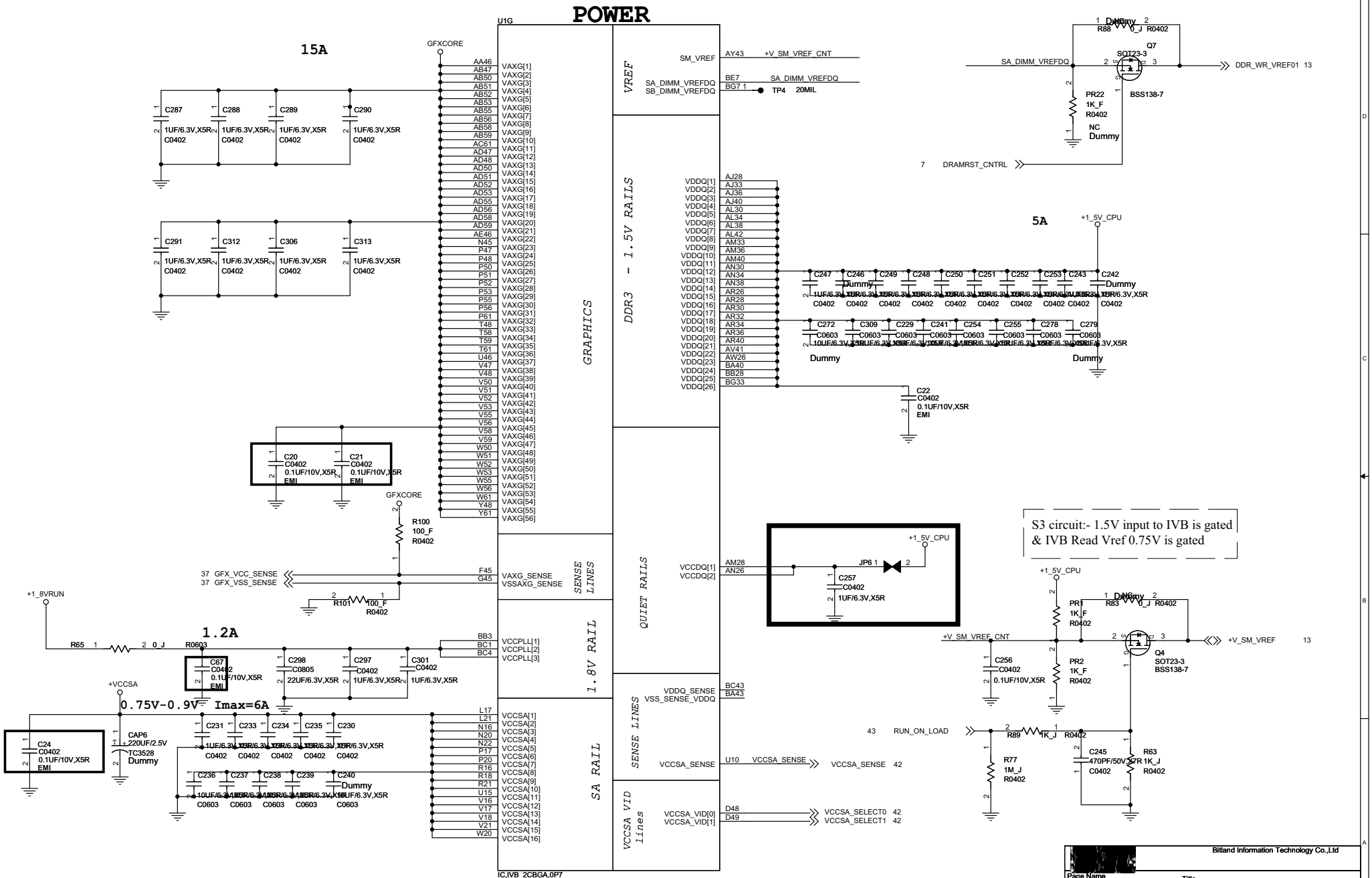
POWER



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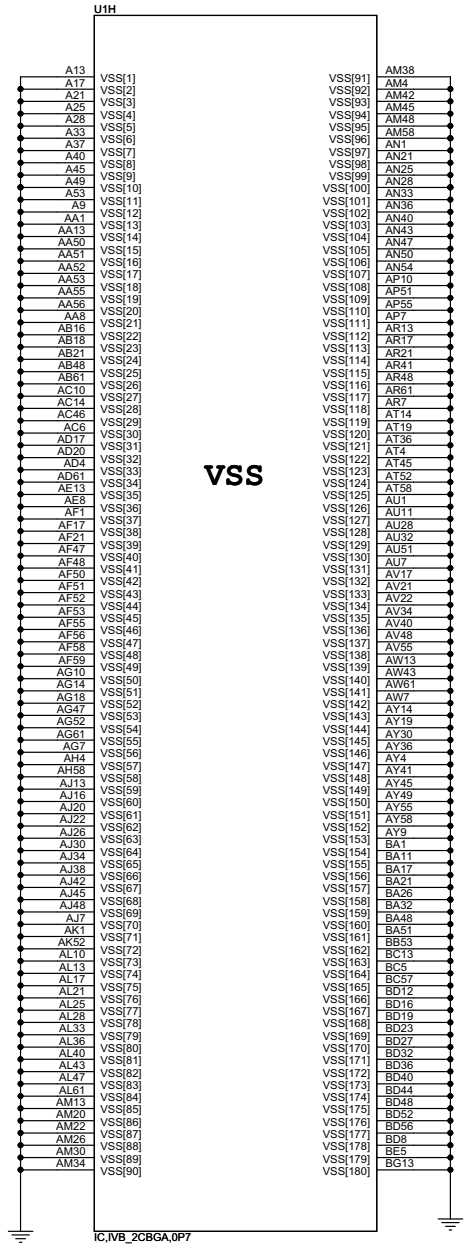

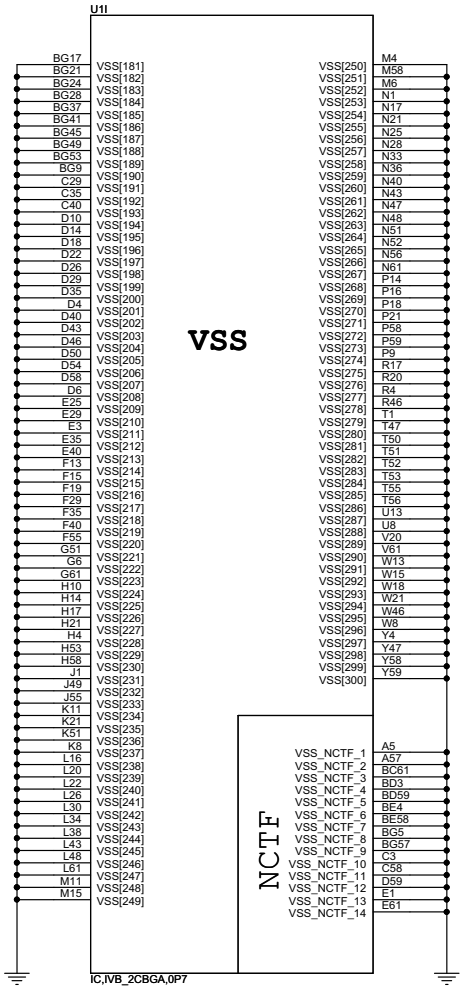

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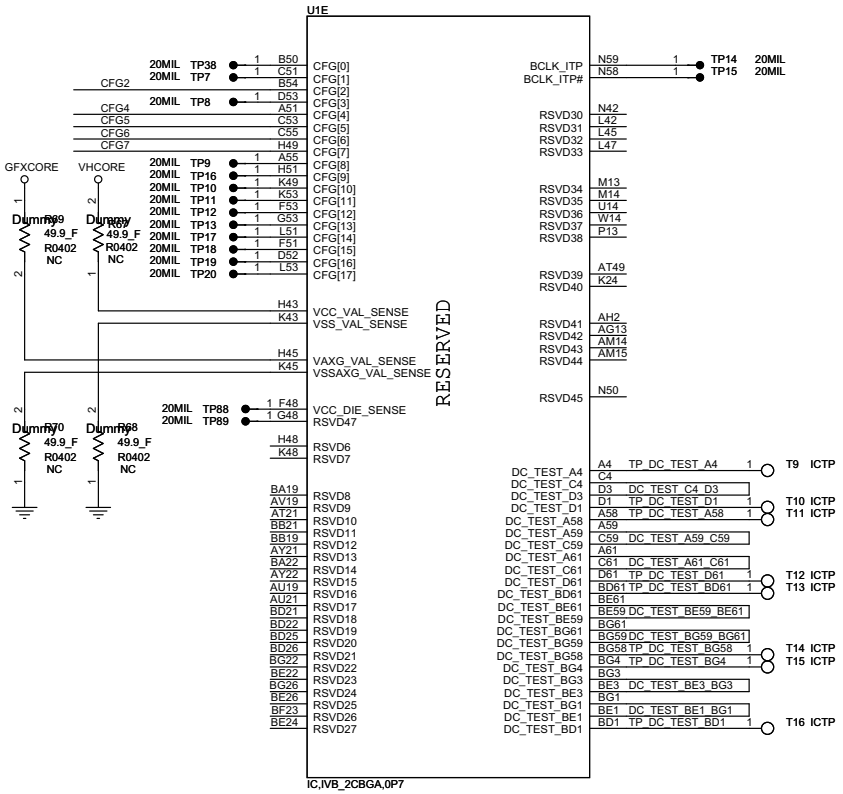
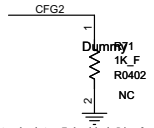
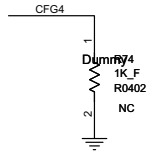


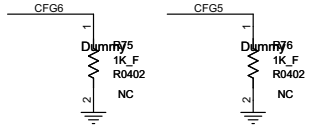
CFG2 1:(Default) Normal Operation; Lane # definition matches socket pin map definition
CFG2 0:Lane Reversed



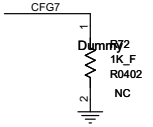
CGF4 1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port
CGF4 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CGF[6: 5]
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



CFG7 1: (Default) PEG Train immediately following xxRESETB de assertion
CFG7 0: PEG Wait for BIOS for training



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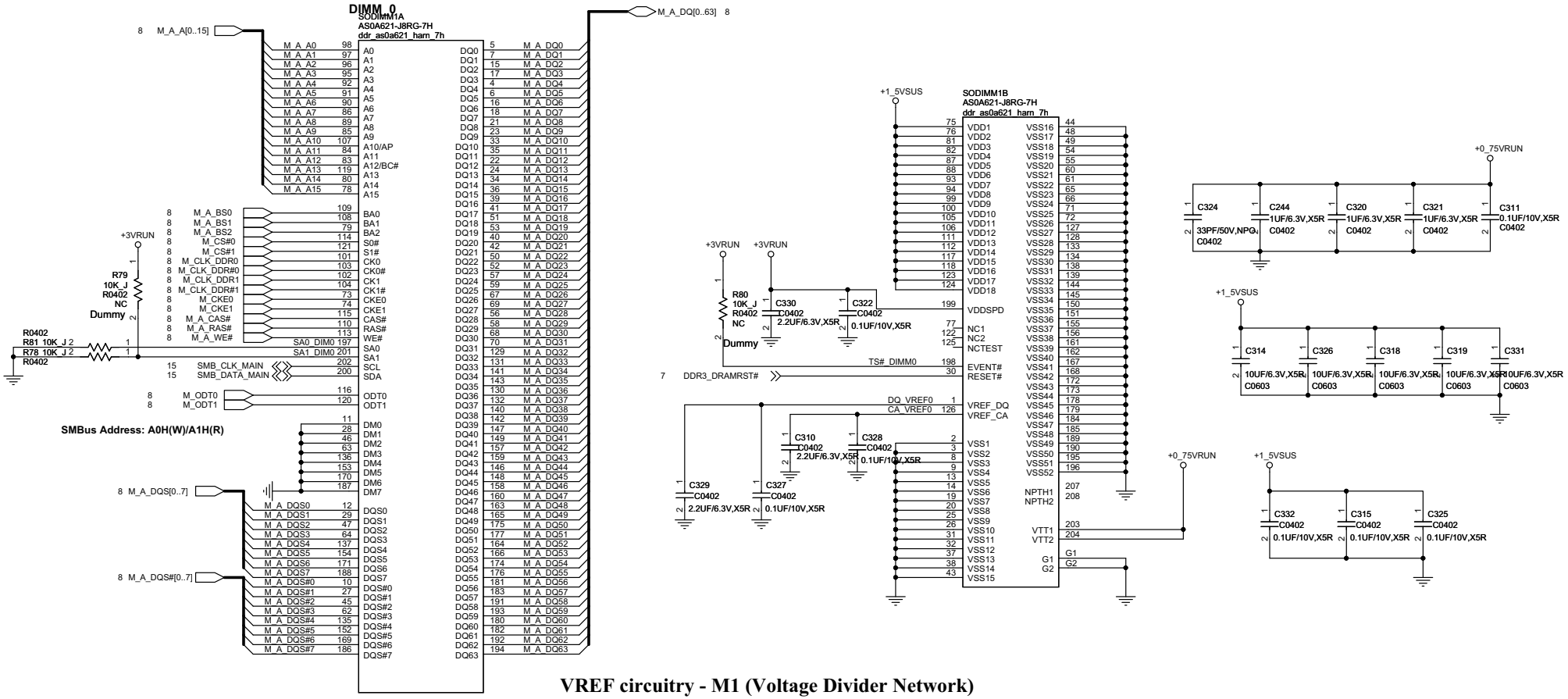
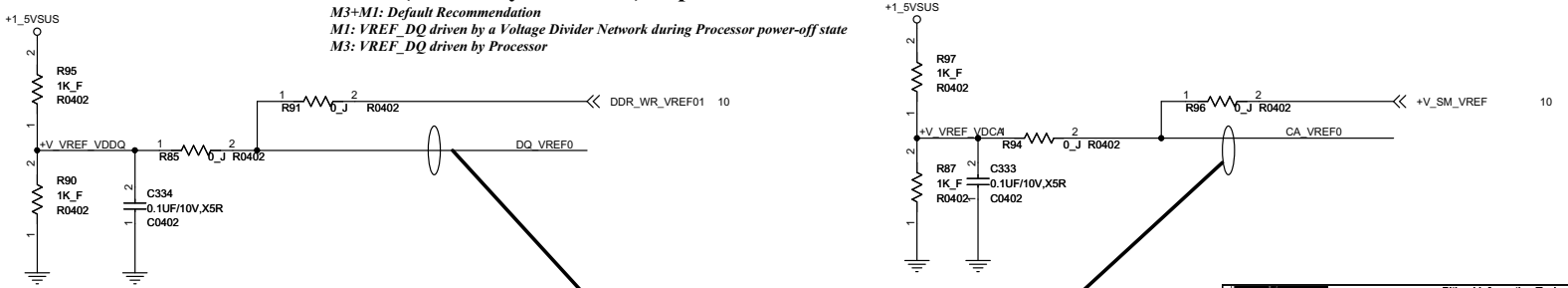


VREF circuitry - M1 (Voltage Divider Network) & M3 (Driven By Processor) implementation

M3+M1: Default Recommendation
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off state
M3: VREF_DQ driven by Processor



CAD NOTE:All VREF traces should be at least 20 mils wide and 20 mils spacing to other signals/planes

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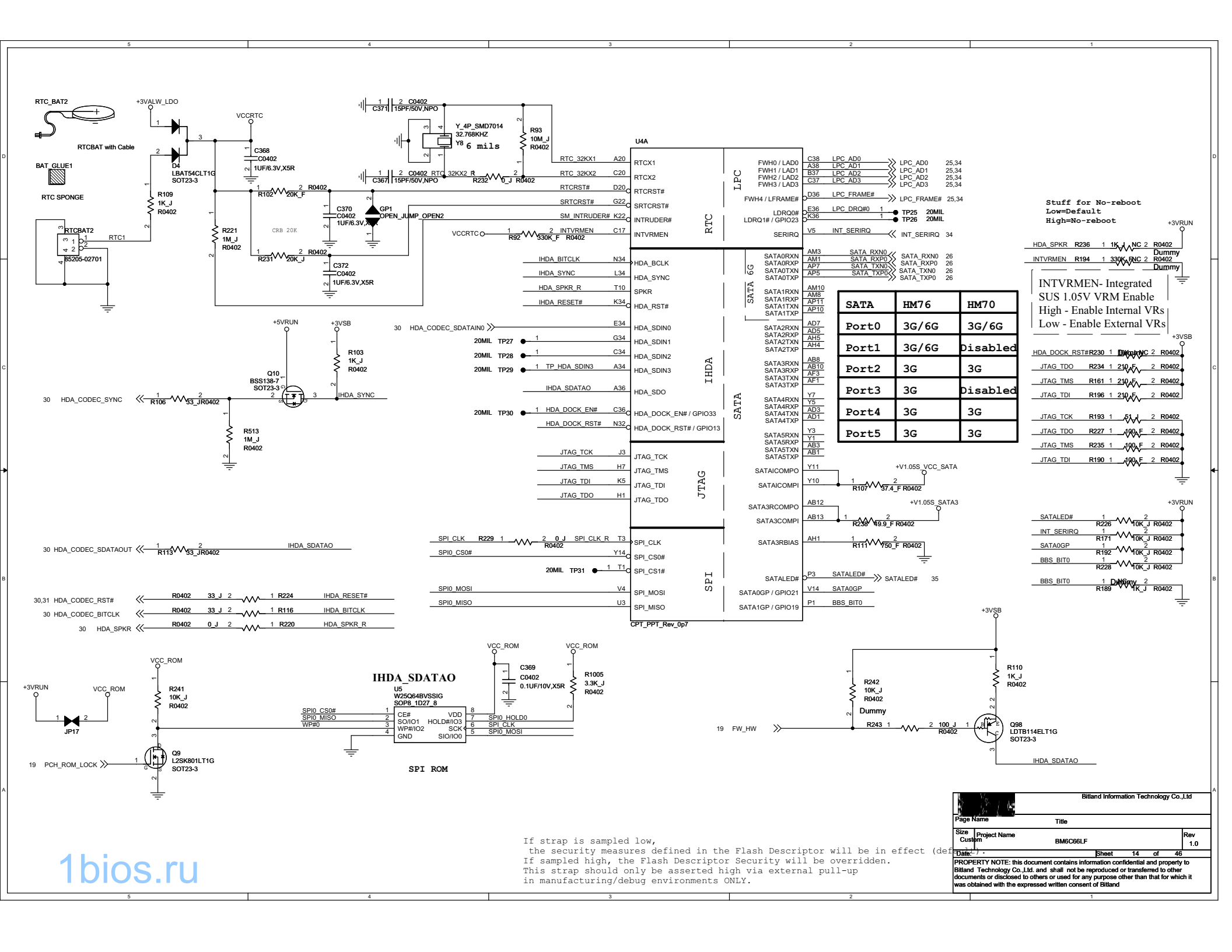
RTC_BAT2
RTCBAT with Cable
BAT_GLUE1
RTC SPONGE
RTCBAT2
B5205-02701
+3VALW_LDO
VCCRTC
D4
LBAT54CLT1G
SOT23-3
R109
1K_J
R0402
R221
1M_J
R0402
C368
C0402
1UF/6.3V,X5R
R102
20K_F
R231
20K_J
C370
C372
GP1
OPEN_JUMP_OPEN2
C371
15PF/50V,NPO
C367
Y_4P_SMD7014
32.768KHZ
Y8
6 mils
R93
10M_J
R232
0_J
RTC1
CRB 20K
U4A
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
RTC
LPC
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
LDRQ1# / GPIO23
SERIRQ
TP25
TP26
20MIL
Stuff for No-reboot
Low=Default
High=No-reboot
INTVRMEN- Integrated
SUS 1.05V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs
IHDA_BITCLK
IHDA_SYNC
HDA_SPKR_R
IHDA_RESET#
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33
HDA_DOCK_RST# / GPIO13
IHDA
SATA
SATA 6G
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA | HM76 | HM70
Port0 | 3G/6G | 3G/6G
Port1 | 3G/6G | Disabled
Port2 | 3G | 3G
Port3 | 3G | Disabled
Port4 | 3G | 3G
Port5 | 3G | 3G
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG
SATAICOMPO
SATAICOMPI
SATA3RCOMPO
SATA3COMPI
SATA3RBIAS
SATALED#
SATA0GP / GPIO21
SATA1GP / GPIO19
SATA0GP
BBS_BIT0
+V1.05S_VCC_SATA
+V1.05S_SATA3
SPI_CLK
SPI0_CS0#
SPI_CS1#
SPI0_MOSI
SPI0_MISO
SPI
CPT_PPT_Rev_0p7
HDA_CODEC_SDATAIN0
HDA_CODEC_SYNC
HDA_CODEC_SDATAOUT
HDA_CODEC_RST#
HDA_CODEC_BITCLK
HDA_SPKR
HDA_SPKR_R
HDA_DOCK_RST#
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
Q10
BSS138-7
SOT23-3
+5VRUN
+3VSB
+3VRUN
R103
1K_J
R0402
R106
33_J
R513
1M_J
R113
R224
R116
R220
R229
R107
57.4_F
R238
49.9_F
R111
750_F
R226
10K_J
R171
R192
R228
R189
IHDA_SDATAO
SPI ROM
U5
W25Q64BVSSIG
SOP8_1D27_8
CE#
SO/IO1
WP#/IO2
GND
VDD
HOLD#/IO3
SCK
SIO/IO0
SPI0_HOLD0
SPI_CLK
SPI0_MOSI
C369
C0402
0.1UF/10V,X5R
R1005
3.3K_J
R0402
VCC_ROM
R241
10K_J
R0402
JP17
Q9
L2SK801LT1G
SOT23-3
PCH_ROM_LOCK
FW_HW
R242
10K_J
R0402
Dummy
R243
100_J
R110
1K_J
Q98
LDTB114ELT1G
SOT23-3
If strap is sampled low,
the security measures defined in the Flash Descriptor will be in effect (default).
If sampled high, the Flash Descriptor Security will be overridden.
This strap should only be asserted high via external pull-up
in manufacturing/debug environments ONLY.
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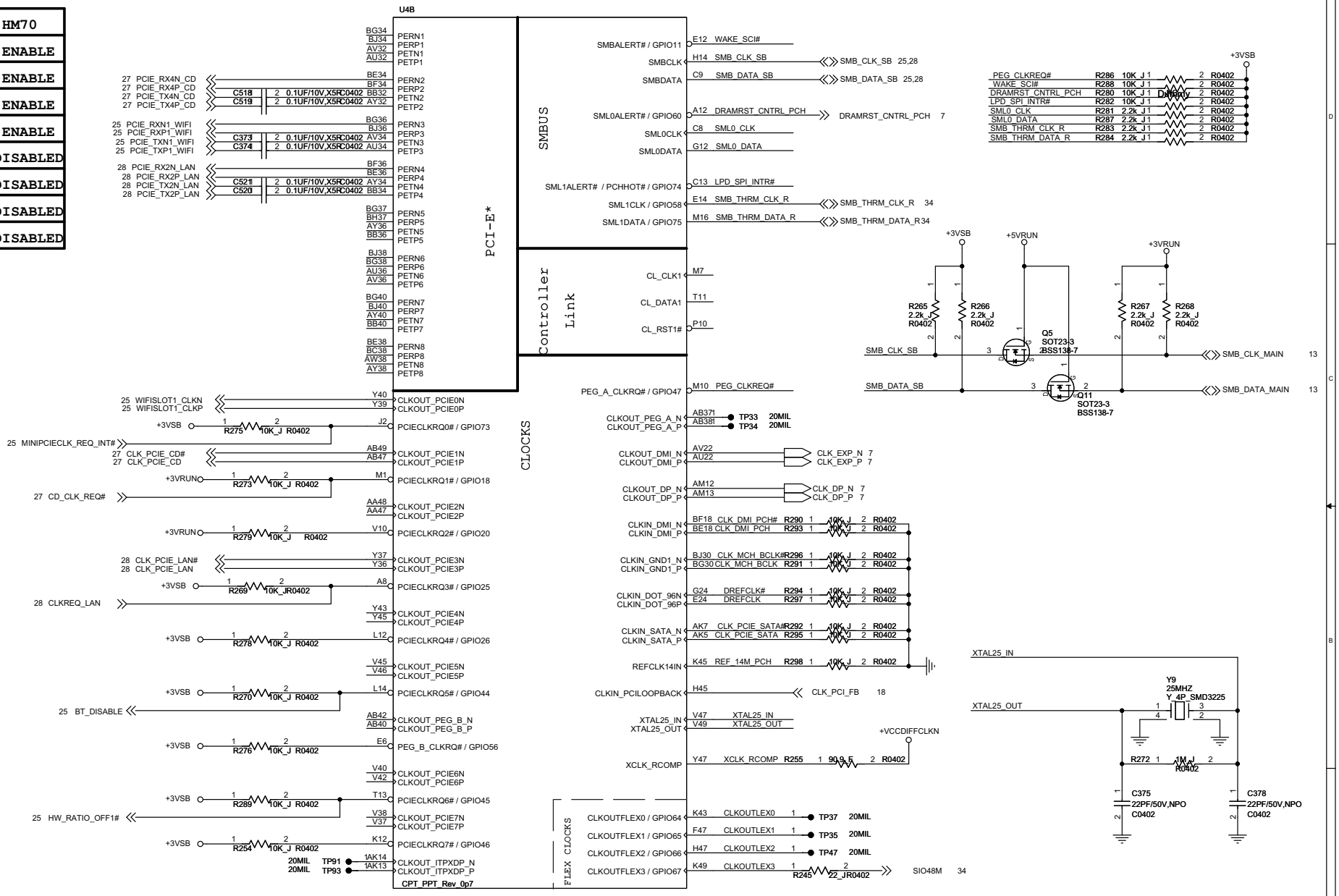
PCIE	HM76	HM70
Port1	ENABLE	ENABLE
Port2	ENABLE	ENABLE
Port3	ENABLE	ENABLE
Port4	ENABLE	ENABLE
Port5	ENABLE	DISABLED
Port6	ENABLE	DISABLED
Port7	ENABLE	DISABLED
Port8	ENABLE	DISABLED



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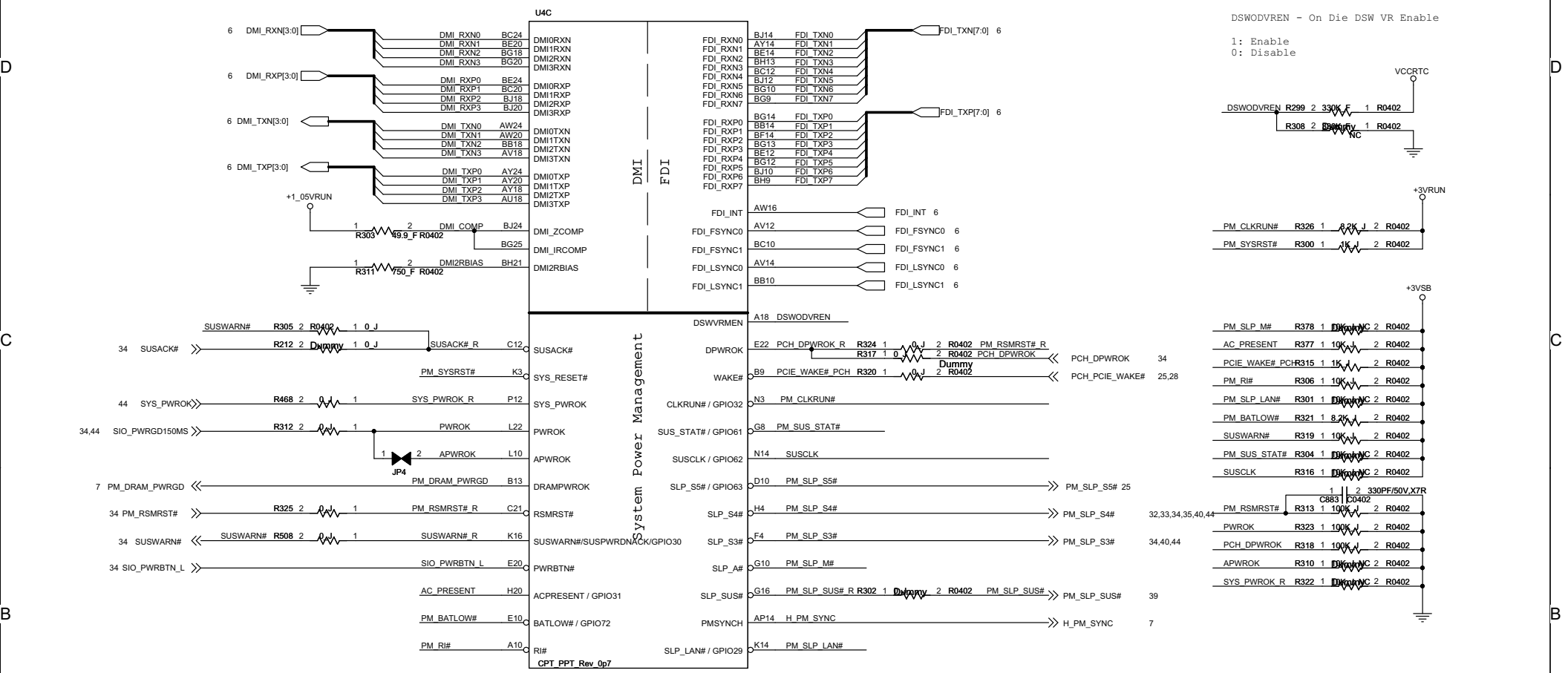

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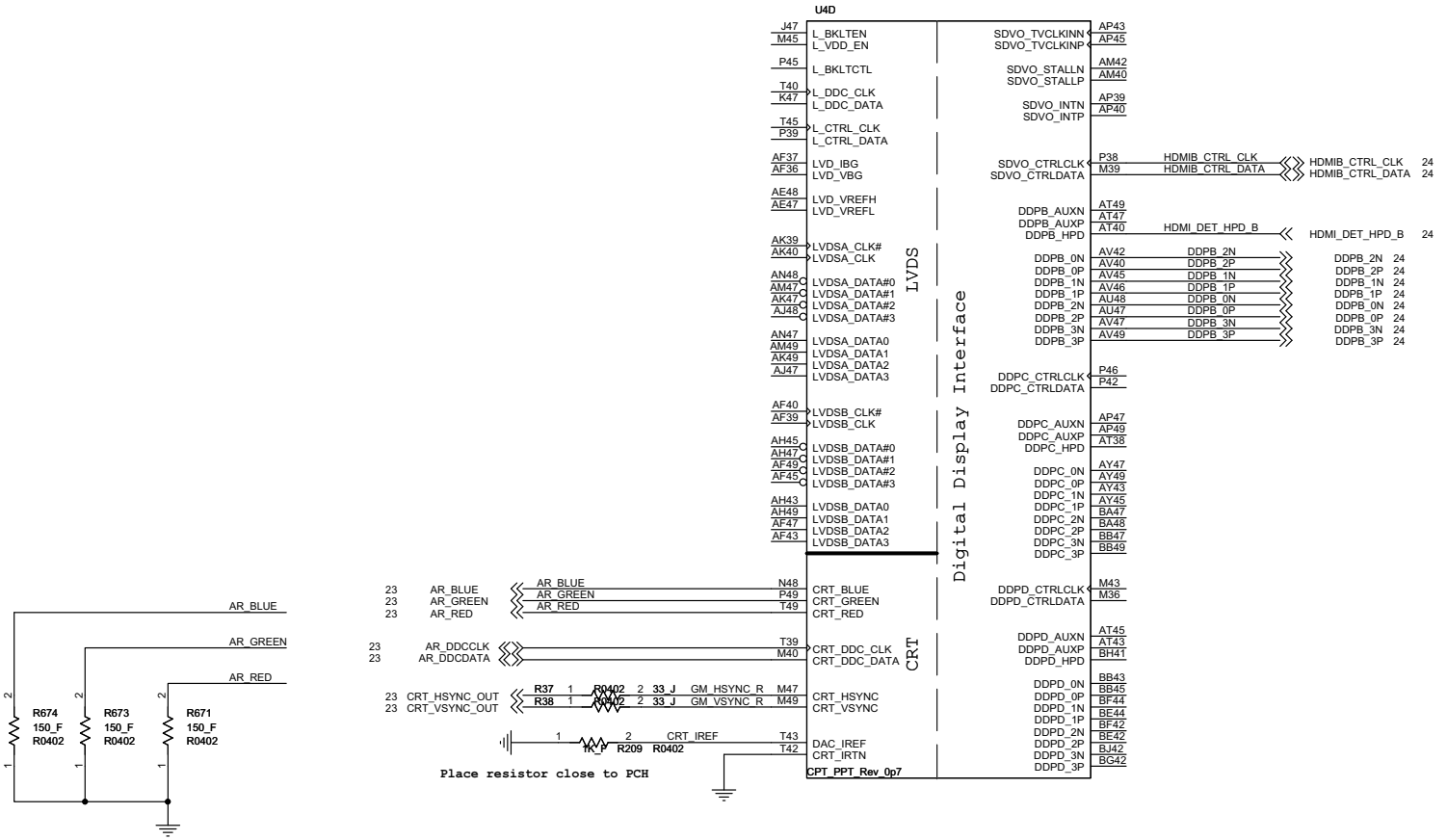

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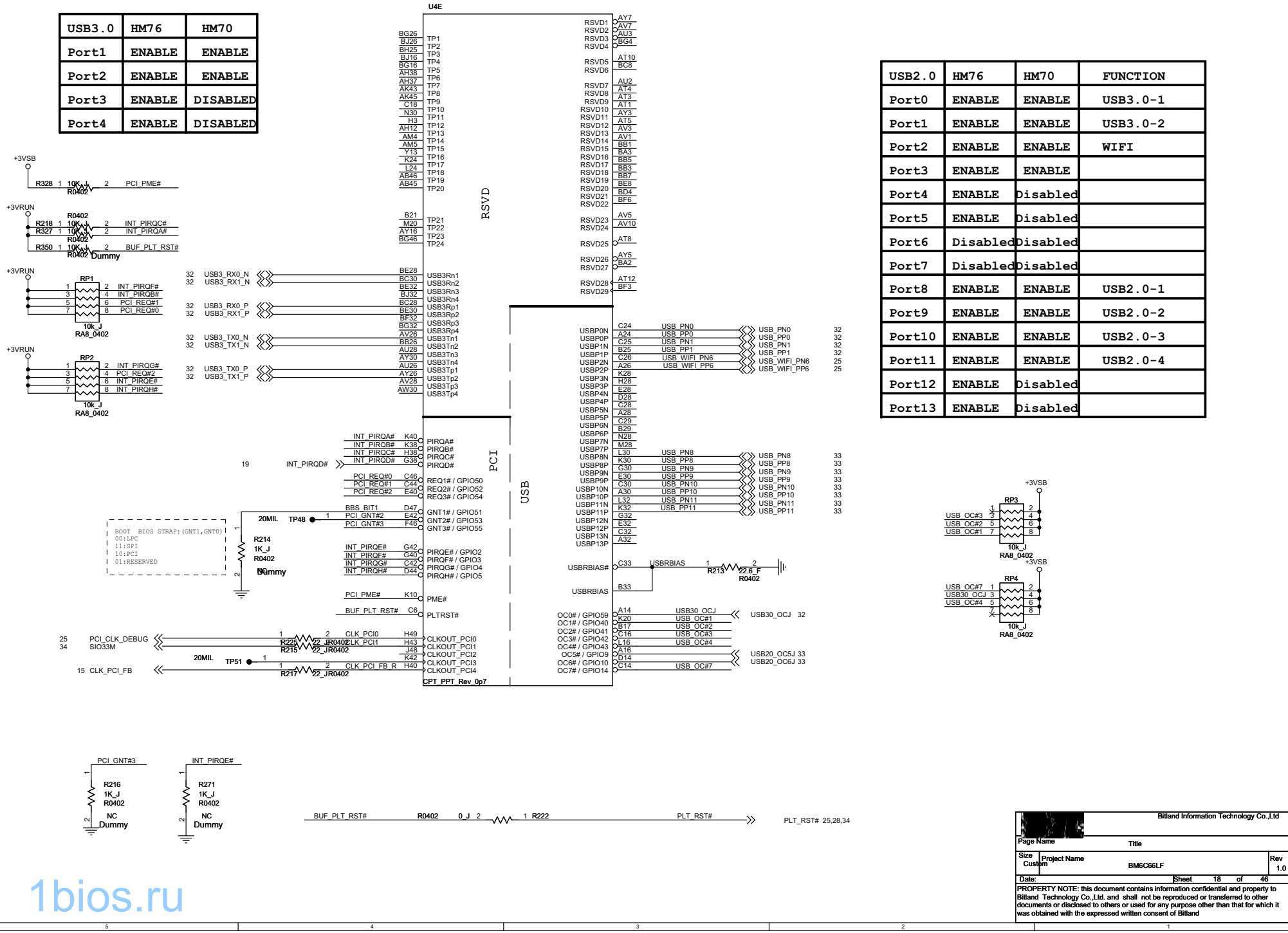
USB3.0	HM76	HM70
Port1	ENABLE	ENABLE
Port2	ENABLE	ENABLE
Port3	ENABLE	DISABLED
Port4	ENABLE	DISABLED

USB2.0	HM76	HM70	FUNCTION
Port0	ENABLE	ENABLE	USB3.0-1
Port1	ENABLE	ENABLE	USB3.0-2
Port2	ENABLE	ENABLE	WIFI
Port3	ENABLE	ENABLE	
Port4	ENABLE	Disabled	
Port5	ENABLE	Disabled	
Port6	Disabled	Disabled	
Port7	Disabled	Disabled	
Port8	ENABLE	ENABLE	USB2.0-1
Port9	ENABLE	ENABLE	USB2.0-2
Port10	ENABLE	ENABLE	USB2.0-3
Port11	ENABLE	ENABLE	USB2.0-4
Port12	ENABLE	Disabled	
Port13	ENABLE	Disabled	



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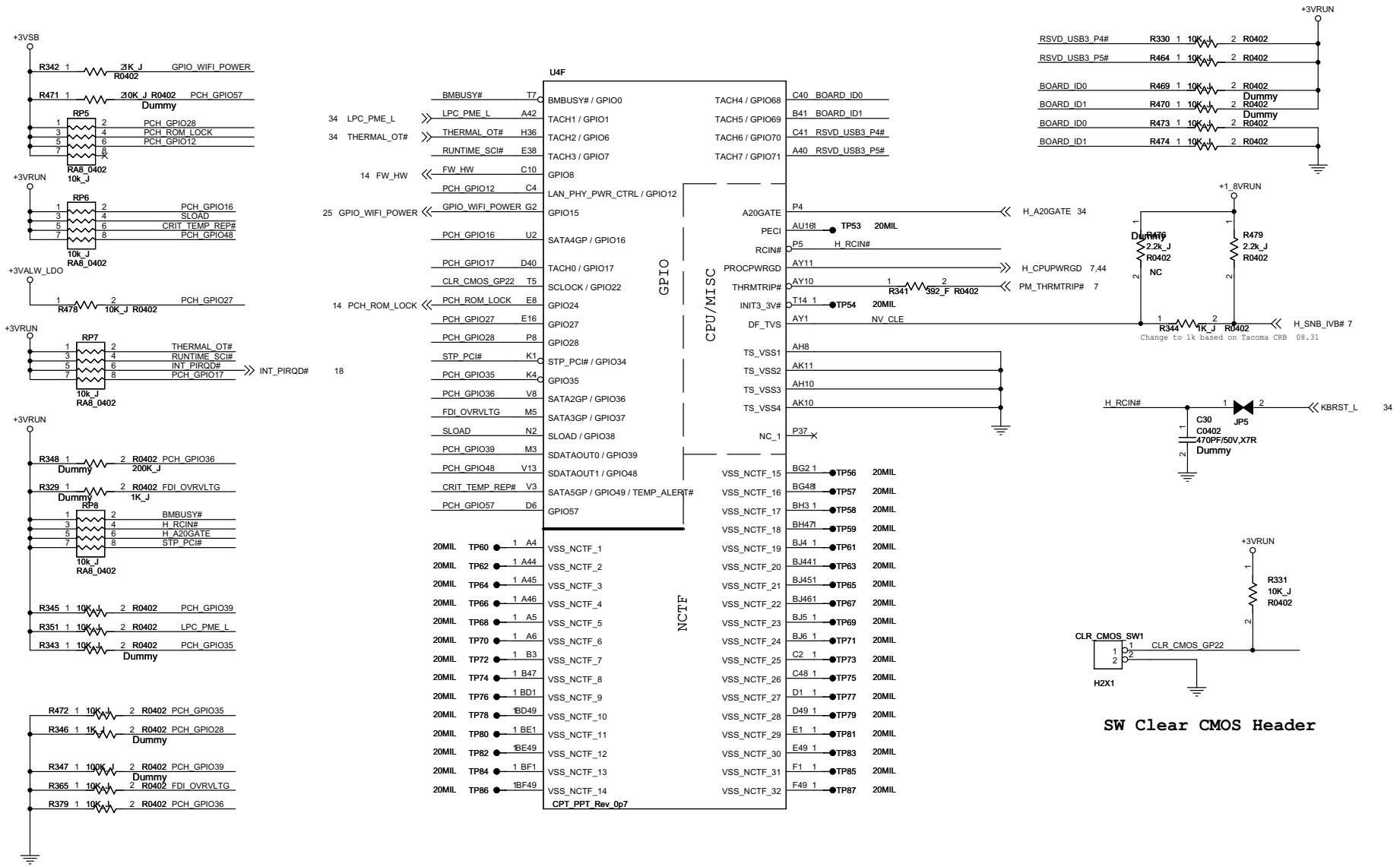

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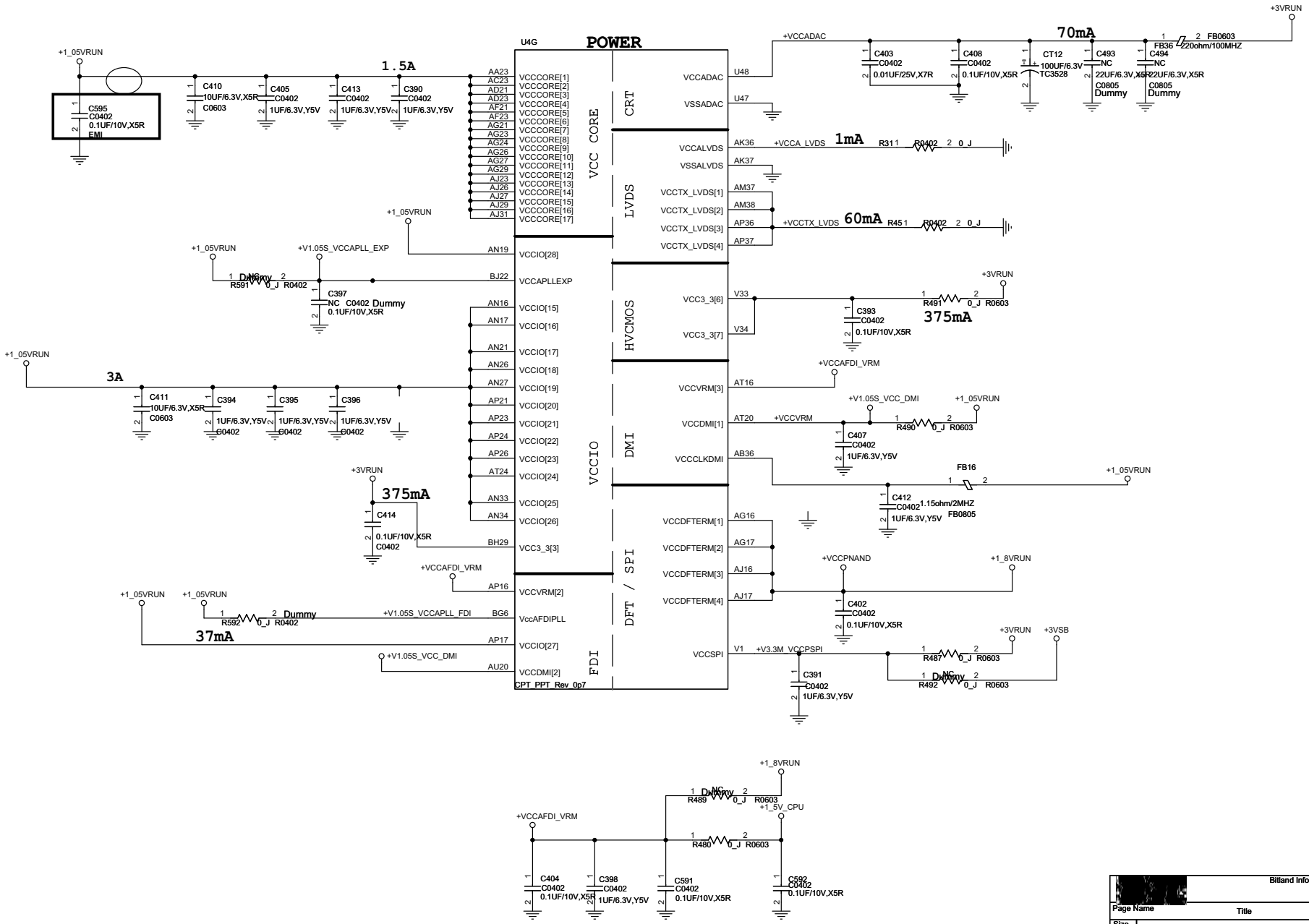

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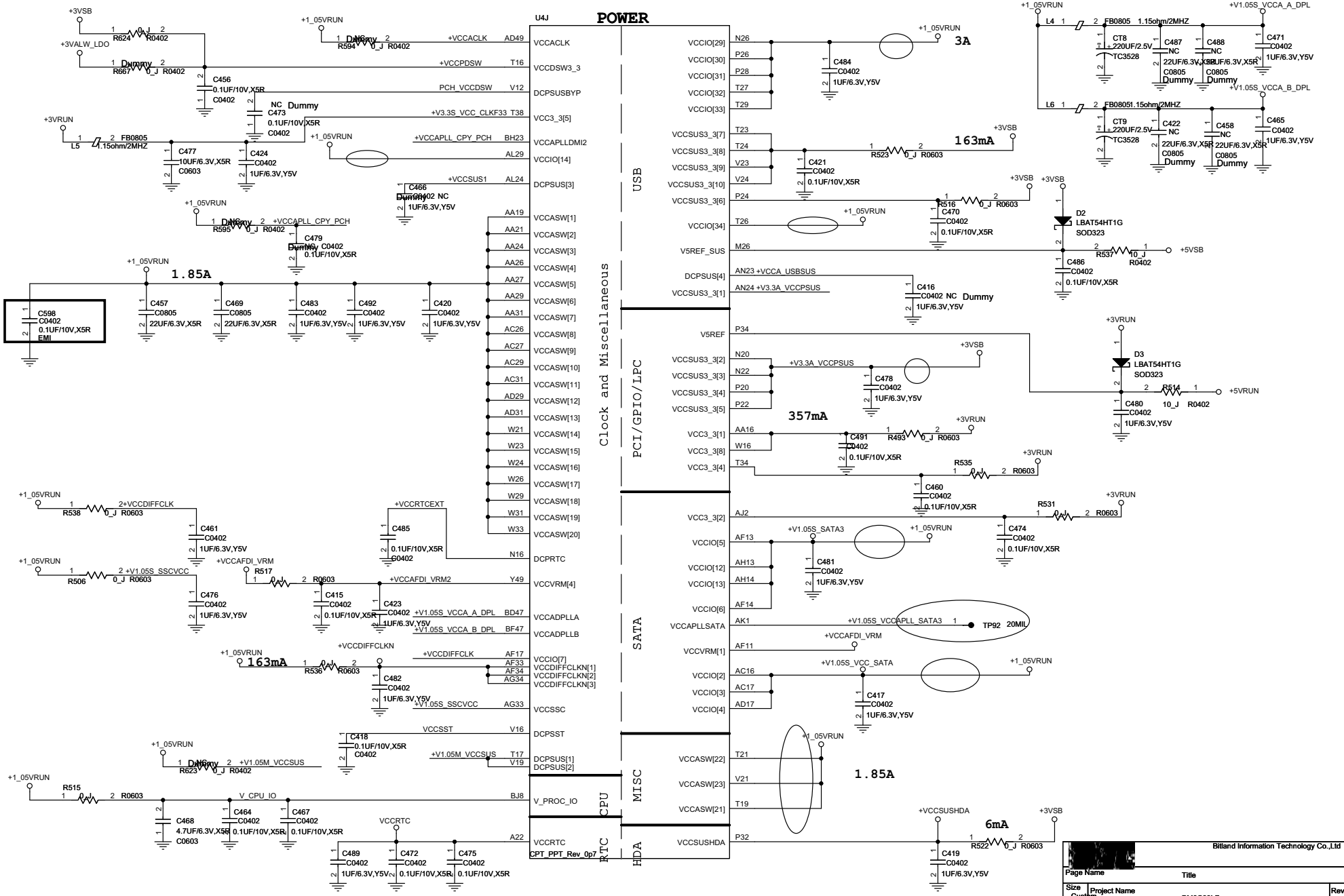
POWER
U4J
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
MISC
CPU
RTC
HDA
VCCACLK
VCCDSW3_3
DCPSUSBYP
VCC3_3[5]
VCCAPLLDMI2
VCCIO[14]
DCPSUS[3]
VCCASW[1]
VCCASW[2]
VCCASW[3]
VCCASW[4]
VCCASW[5]
VCCASW[6]
VCCASW[7]
VCCASW[8]
VCCASW[9]
VCCASW[10]
VCCASW[11]
VCCASW[12]
VCCASW[13]
VCCASW[14]
VCCASW[15]
VCCASW[16]
VCCASW[17]
VCCASW[18]
VCCASW[19]
VCCASW[20]
DCPRTC
VCCVRM[4]
VCCADPLLA
VCCADPLLB
VCCIO[7]
VCCDIFFCLKN[1]
VCCDIFFCLKN[2]
VCCDIFFCLKN[3]
VCCSSC
DCPSST
DCPSUS[1]
DCPSUS[2]
V_PROC_IO
VCCRTC
CPT_PPT_Rev_0p7
VCCIO[29]
VCCIO[30]
VCCIO[31]
VCCIO[32]
VCCIO[33]
VCCSUS3_3[7]
VCCSUS3_3[8]
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VCCIO[34]
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VCCIO[13]
VCCIO[6]
VCCAPLLSATA
VCCVRM[1]
VCCIO[2]
VCCIO[3]
VCCIO[4]
VCCASW[22]
VCCASW[23]
VCCASW[21]
VCCSUSHDA
+1_05VRUN
+3VSB
+3VALW_LDO
+3VRUN
+5VSB
+V1.05S_VCCA_A_DPL
+V1.05S_VCCA_B_DPL
+VCCACLK
+VCCPDSW
PCH_VCCDSW
+V3.3S_VCC_CLKF33
+VCCAPLL_CPY_PCH
+VCCSUS1
+V3.3A_VCCPSUS
+VCCA_USBSUS
+V1.05S_SATA3
+V1.05S_VCCAPLL_SATA3
+V1.05S_VCC_SATA
+VCCDIFFCLK
+VCCRTCEXT
+VCCAFDI_VRM
+V1.05S_SSCVCC
+V1.05M_VCCSUS
VCCSST
V_CPU_IO
VCCRTC
3A
163mA
1.85A
357mA
6mA
1.85A
Dummy
NC
EMI
TP92 20MIL
LBAT54HT1G
SOD323
FB0805 1.15ohm/2MHZ
CT8 220UF/2.5V TC3528
CT9 220UF/2.5V TC3528
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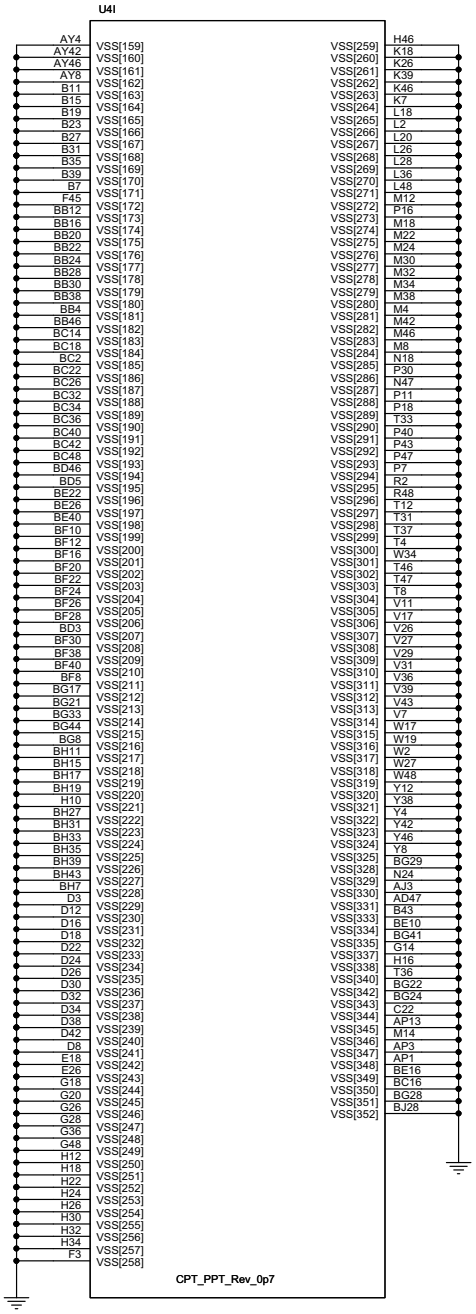

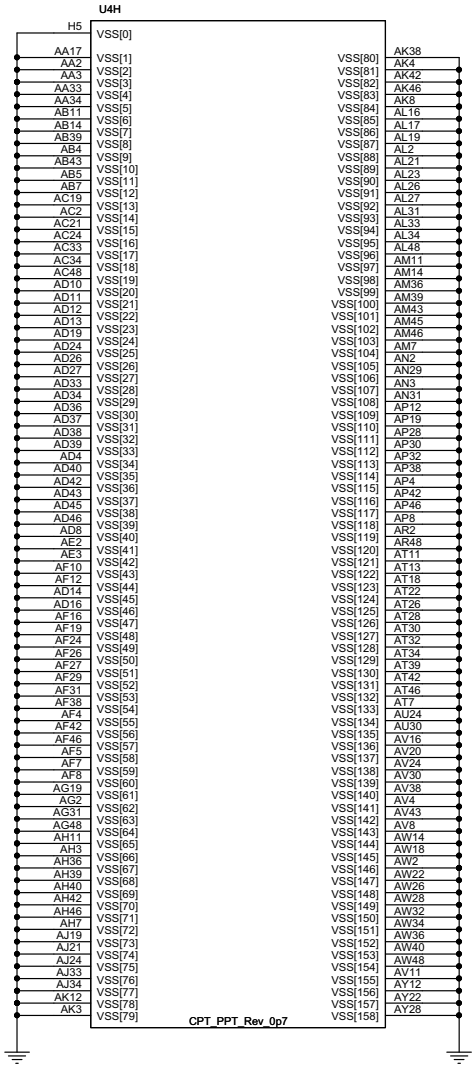

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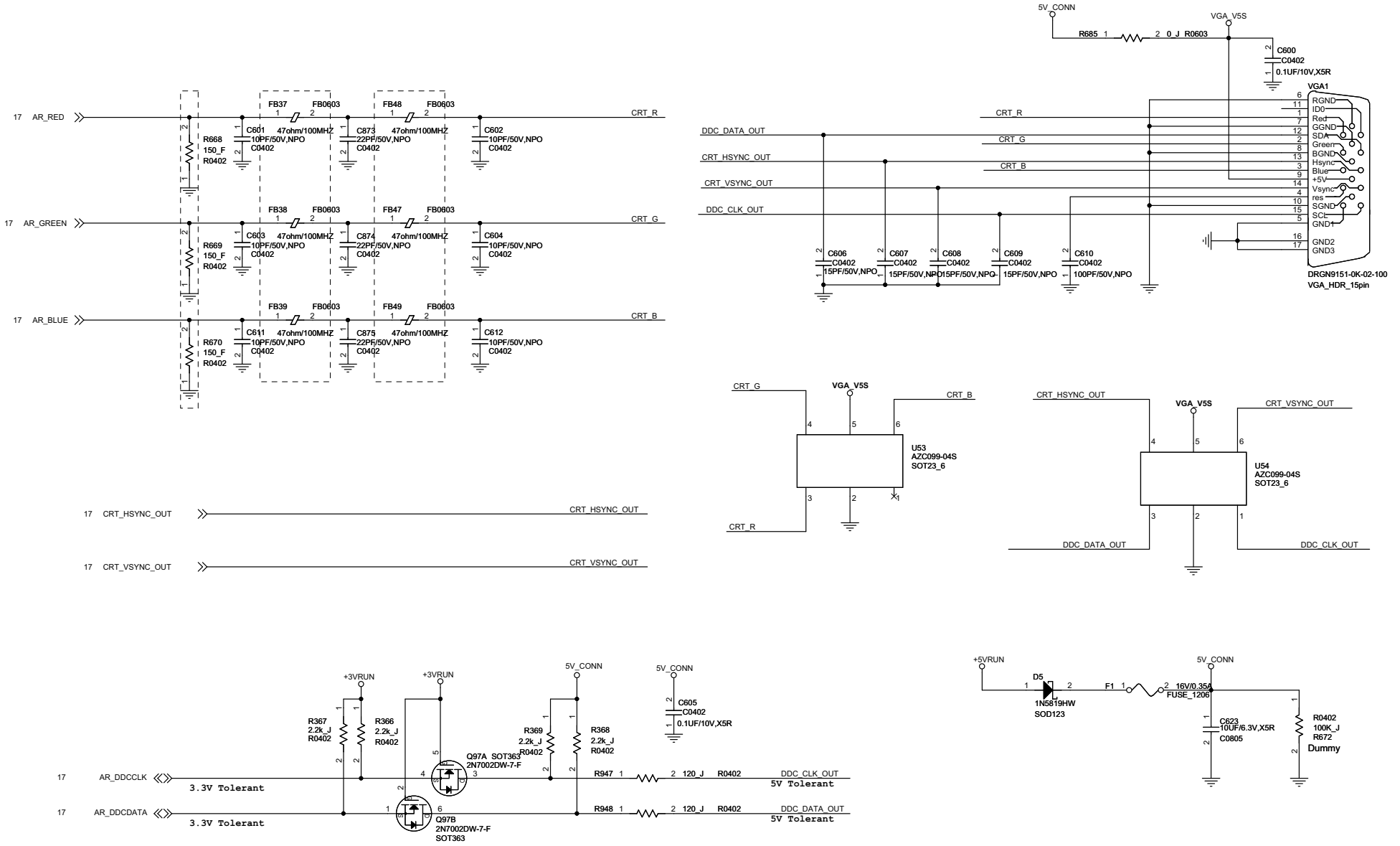

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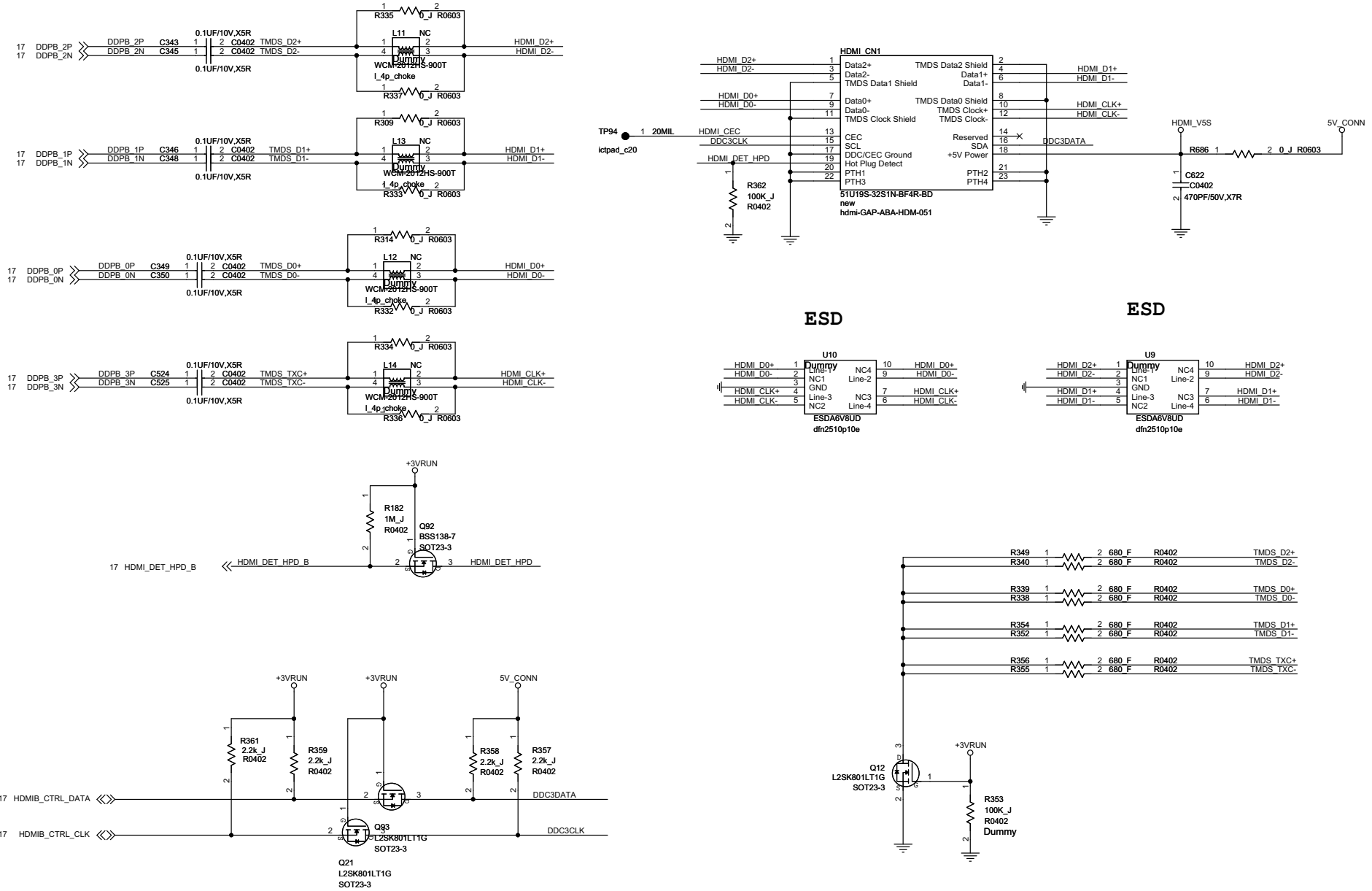

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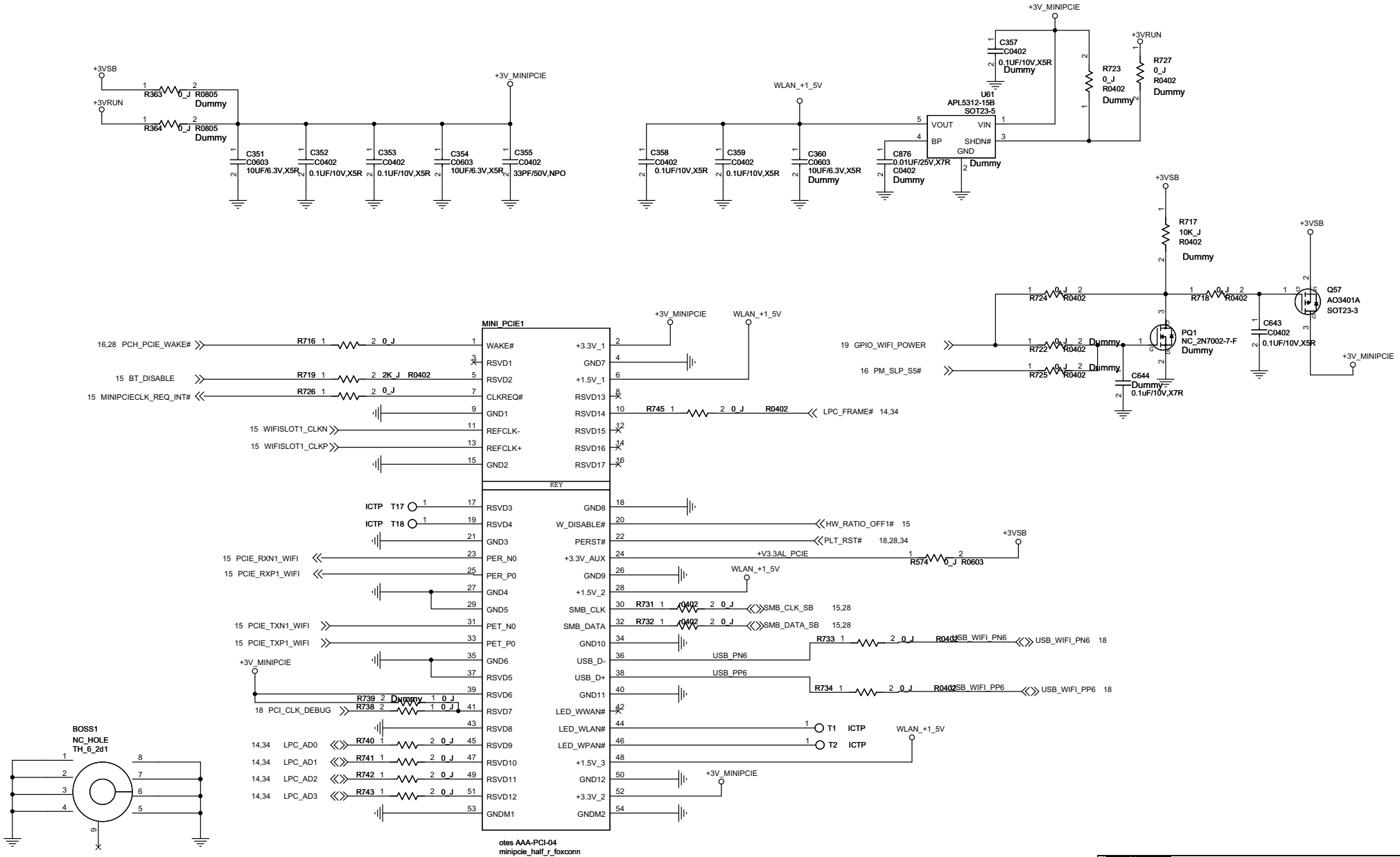

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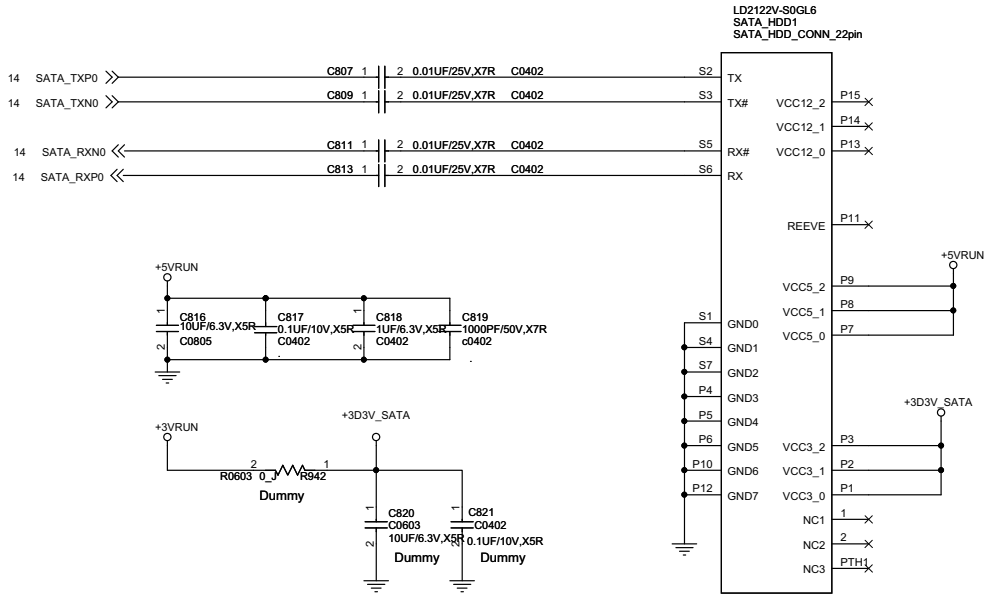

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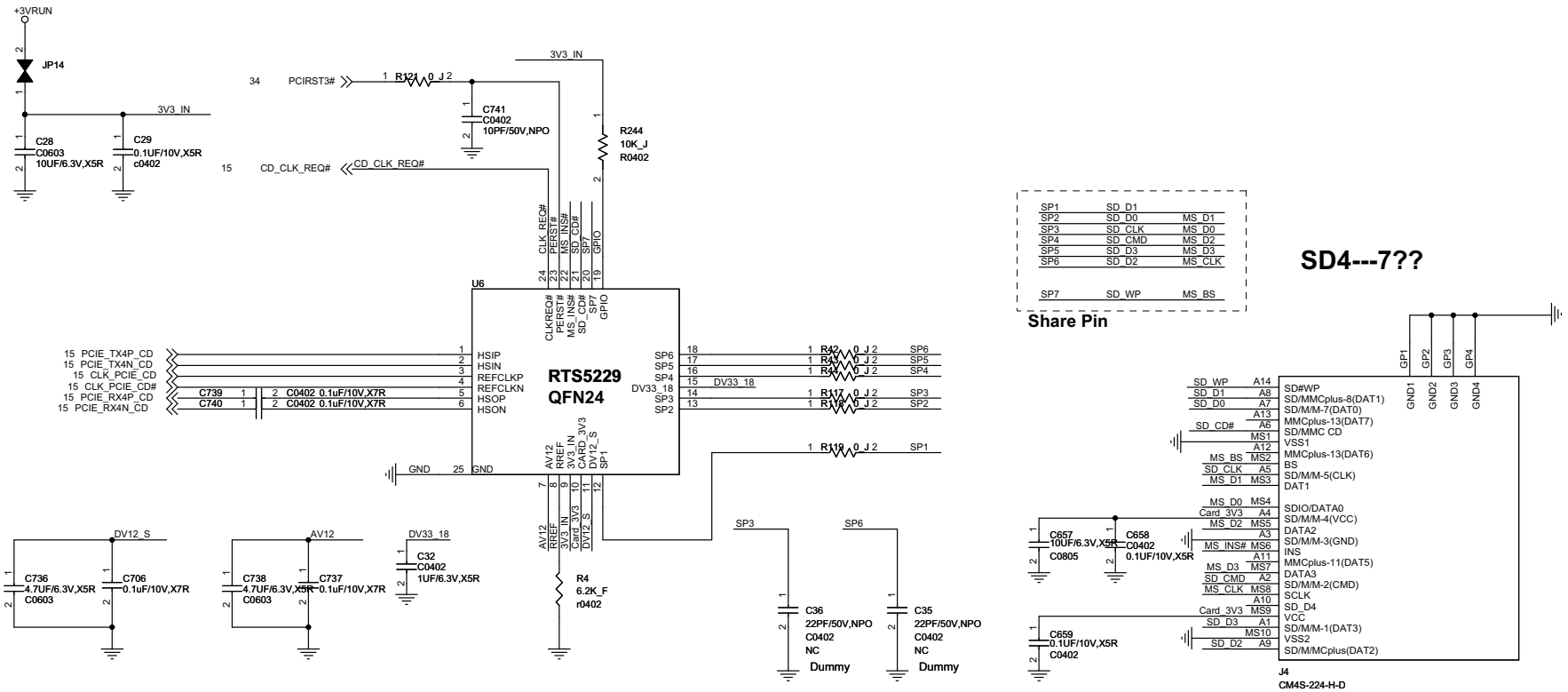

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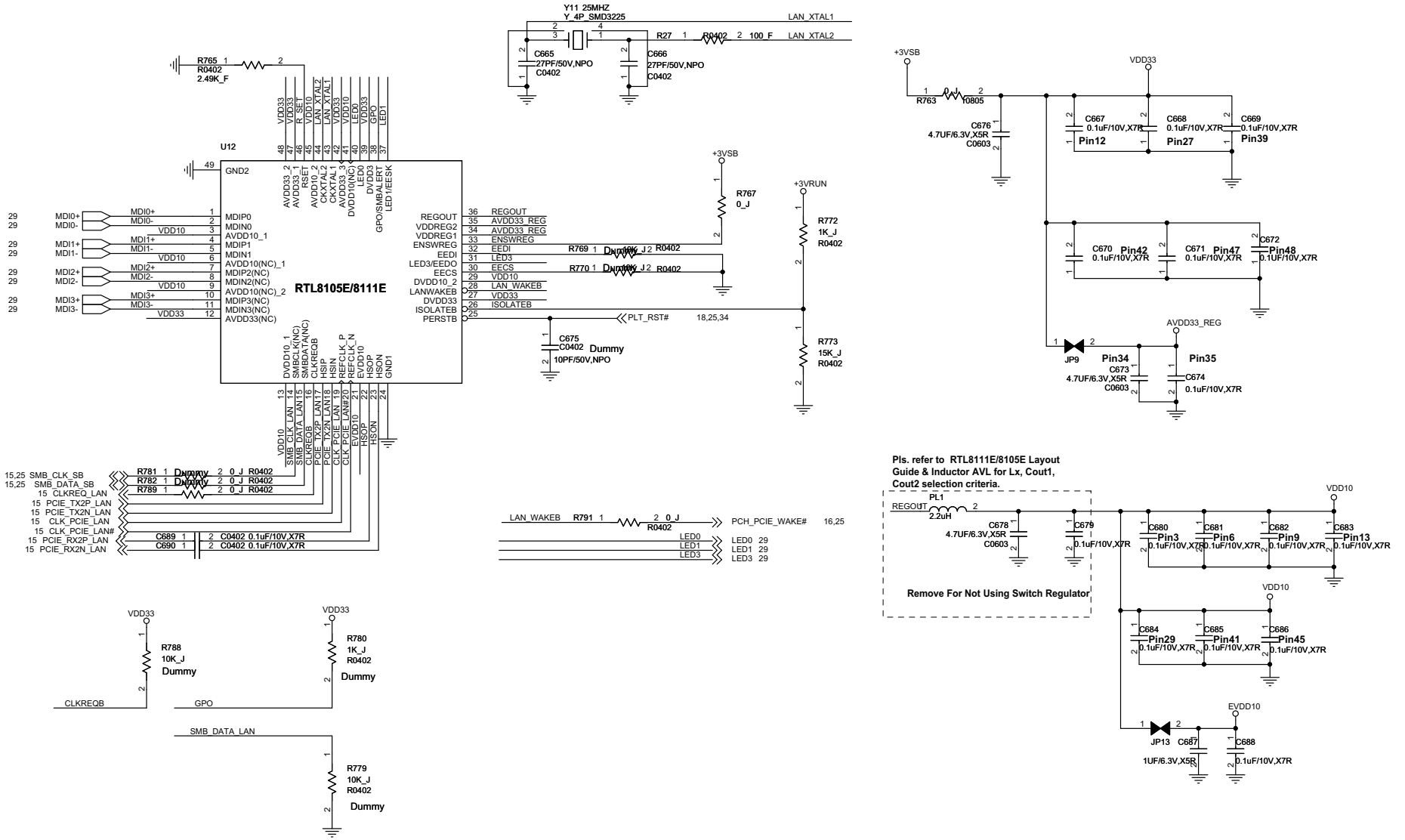

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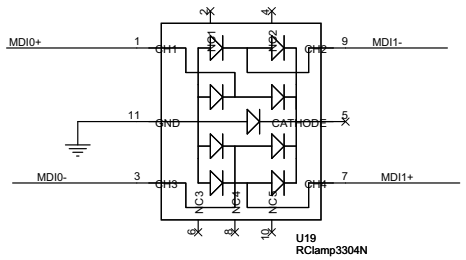

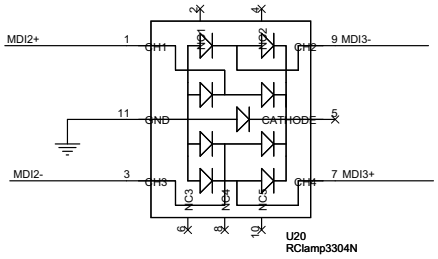

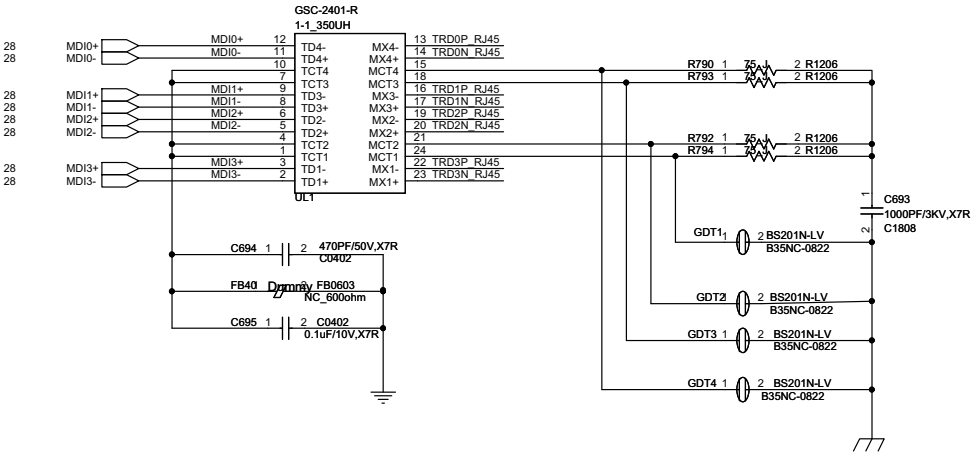

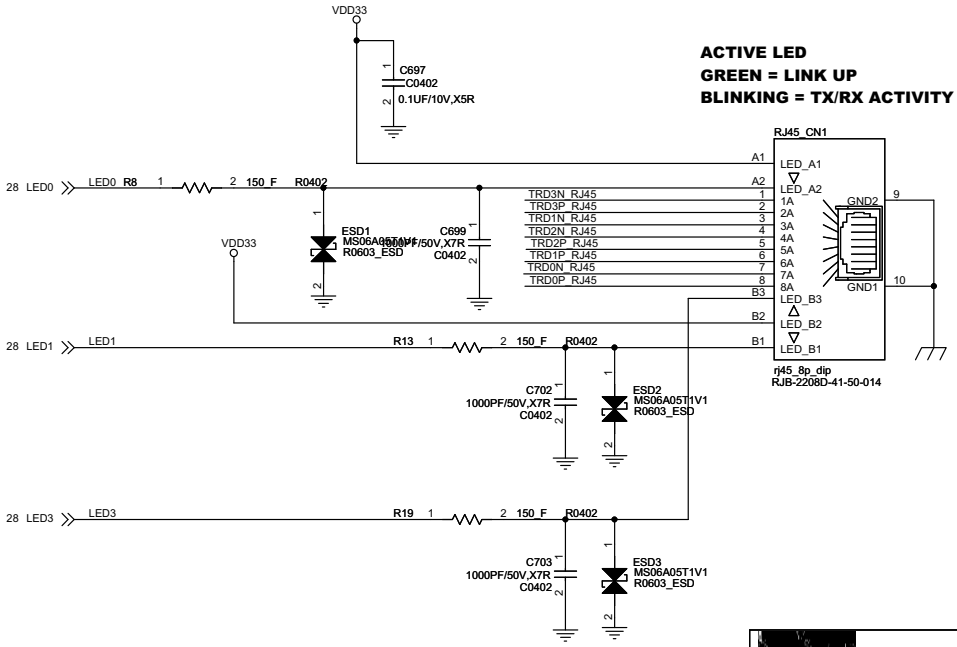

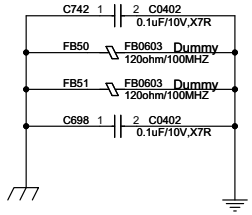

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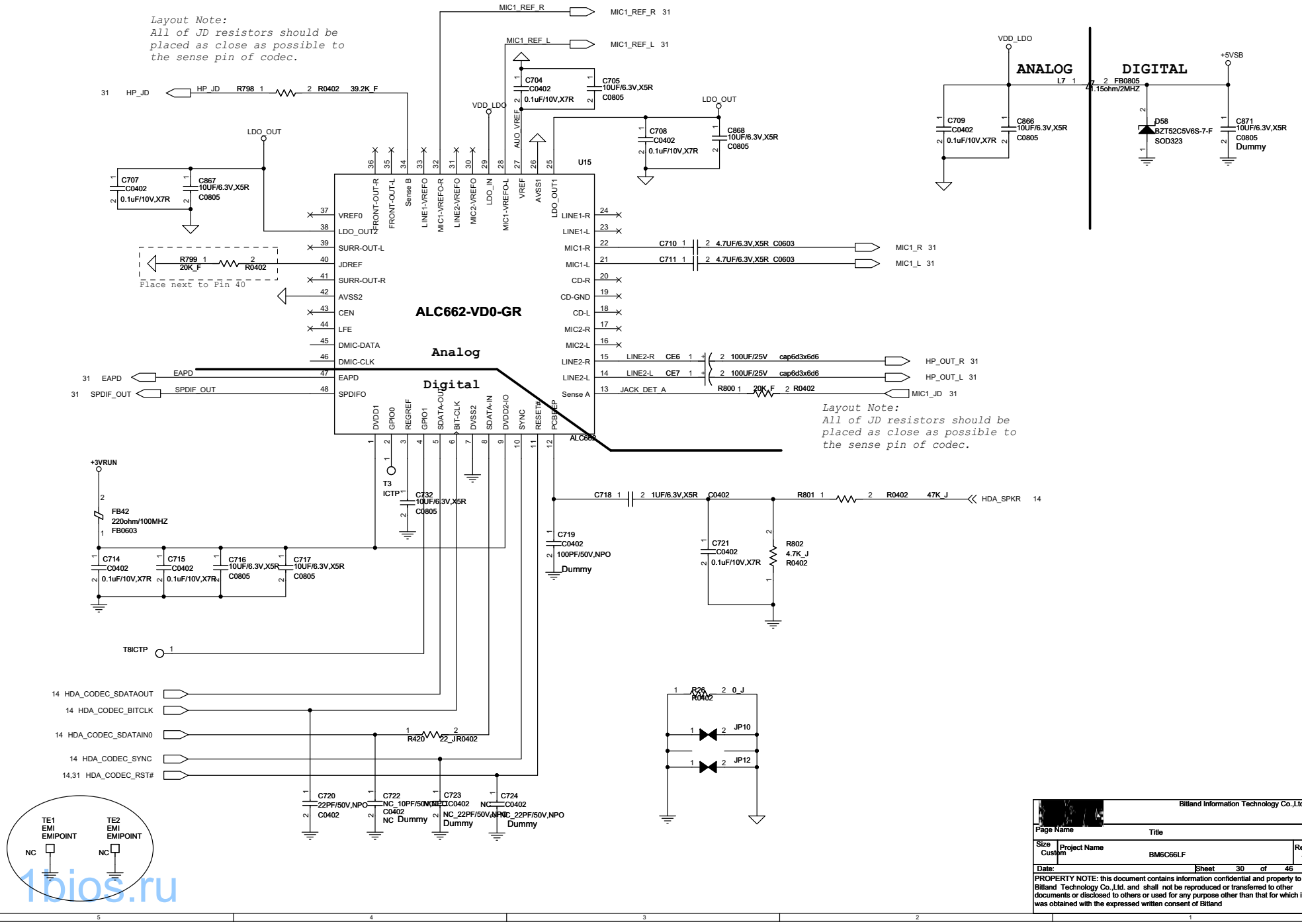

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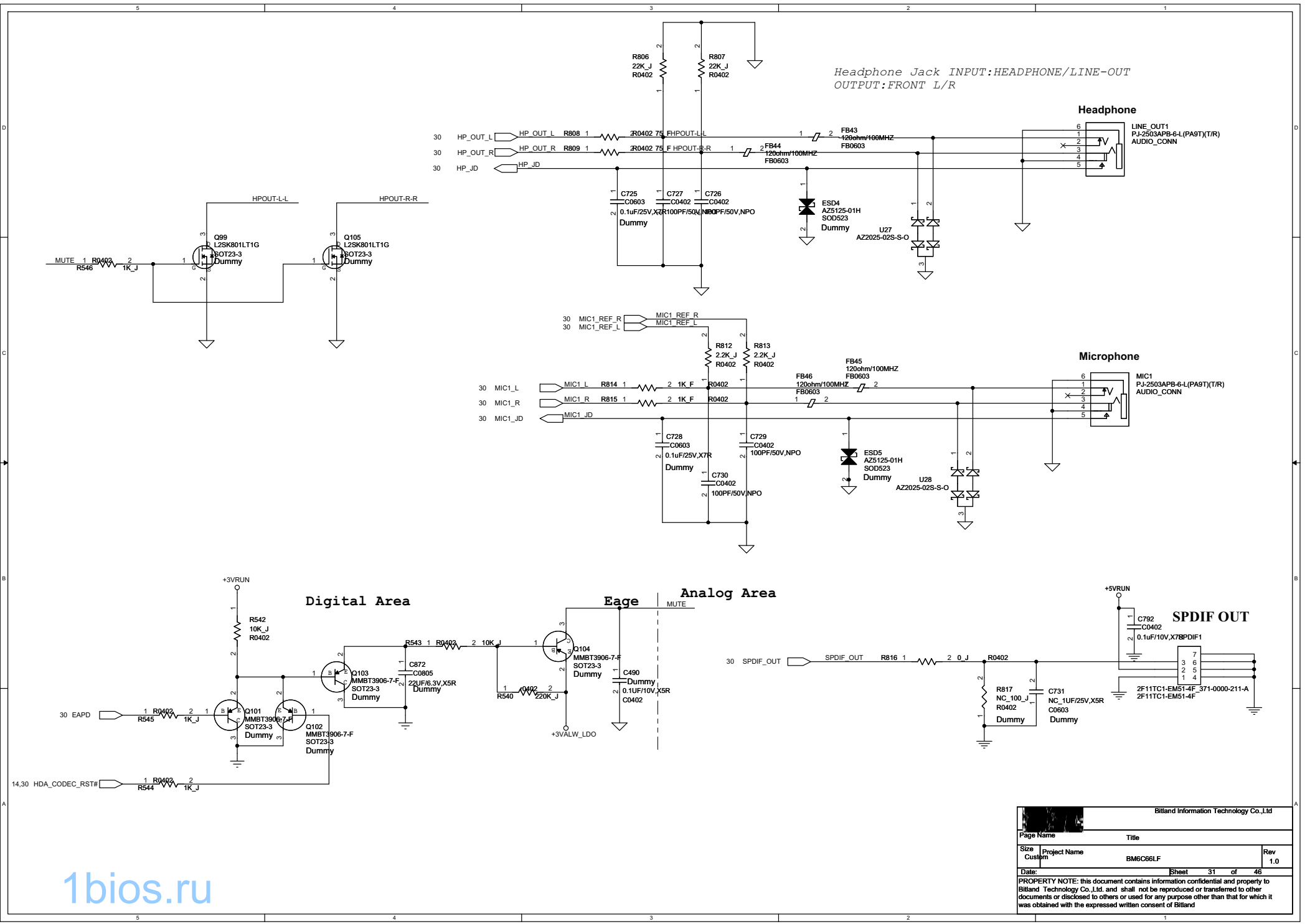
Headphone Jack INPUT:HEADPHONE/LINE-OUT
OUTPUT:FRONT L/R
Headphone
Microphone
Digital Area
Eage
Analog Area
SPDIF OUT
HP_OUT_L
HP_OUT_R
HP_JD
MIC1_REF_R
MIC1_REF_L
MIC1_L
MIC1_R
MIC1_JD
MUTE
EAPD
HDA_CODEC_RST#
SPDIF_OUT
HPOUT-L-L
HPOUT-R-R
+3VRUN
+5VRUN
+3VALW_LDO
LINE_OUT1
PJ-2503APB-6-L(PA9T)(T/R)
AUDIO_CONN
MIC1
SPDIF1
2F11TC1-EM51-4F_371-0000-211-A
2F11TC1-EM51-4F
Q99
Q105
Q101
Q102
Q103
Q104
L2SK801LT1G
MMBT3906-7-F
SOT23-3
Dummy
ESD4
ESD5
AZ5125-01H
SOD523
U27
U28
AZ2025-02S-S-O
FB43
FB44
FB45
FB46
120ohm/100MHZ
FB0603
R806
R807
22K_J
R0402
R542
10K_J
R543
R540
220K_J
R544
1K_J
R545
R546
R812
R813
2.2K_J
R814
R815
1K_F
R816
0_J
R817
NC_100_J
C725
C726
C727
C728
C729
C730
C731
C792
C872
C490
C0603
C0402
C0805
0.1uF/25V,X7R
100PF/50V,NPO
22UF/6.3V,X5R
0.1UF/10V,X5R
NC_1UF/25V,X5R
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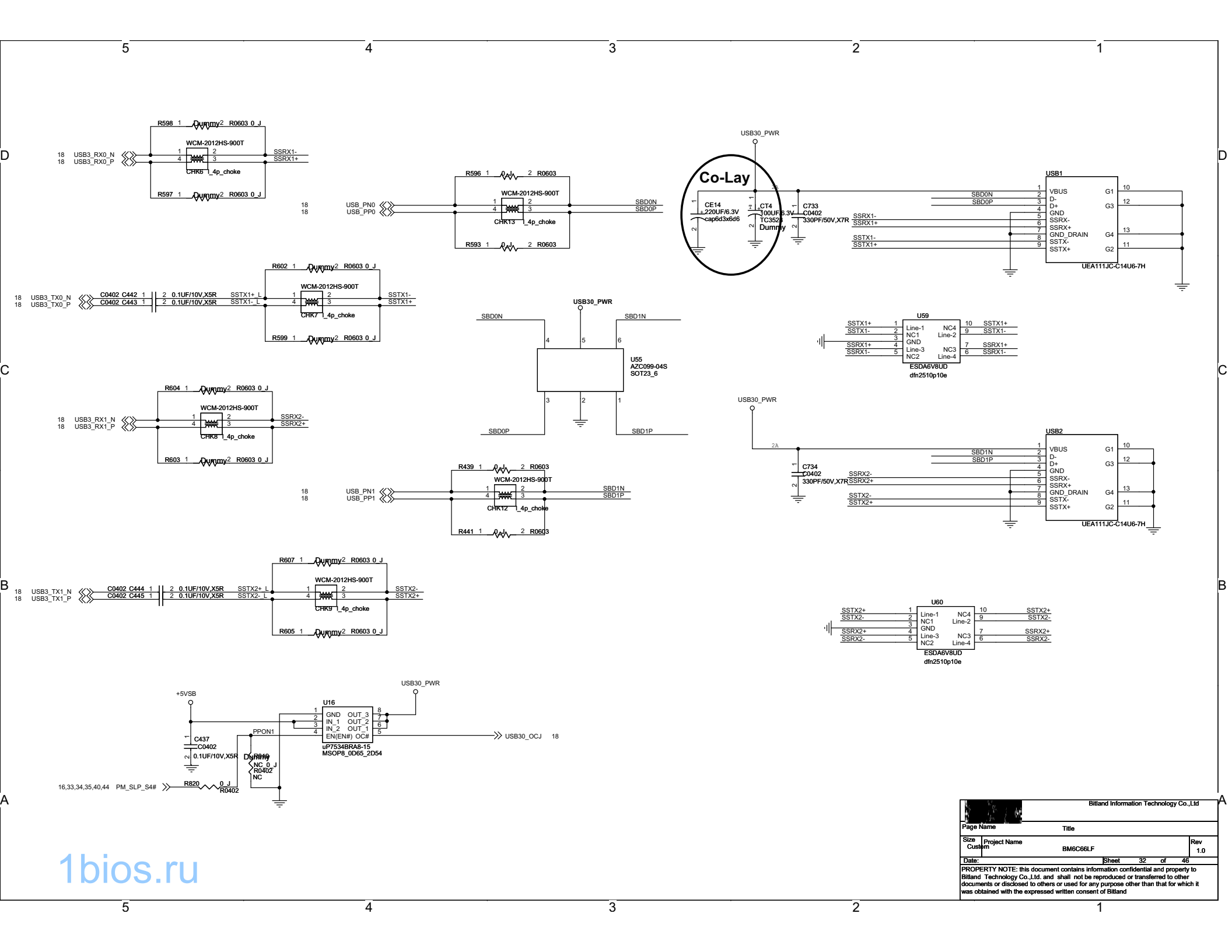
R598 1 Dummy 2 R0603 0_J
WCM-2012HS-900T
18 USB3_RX0_N
18 USB3_RX0_P
SSRX1-
SSRX1+
CHK6 _4p_choke
R597 1 Dummy 2 R0603 0_J
R596 1 0_J 2 R0603
18 USB_PN0
18 USB_PP0
SBD0N
SBD0P
CHK13 _4p_choke
R593 1 0_J 2 R0603
USB30_PWR
Co-Lay
CE14
220UF/6.3V
cap6d3x6d6
CT4
100UF/6.3V
TC352
Dummy
C733
C0402
330PF/50V,X7R
USB1
VBUS
D-
D+
GND
SSRX-
SSRX+
GND_DRAIN
SSTX-
SSTX+
UEA111JC-C14U6-7H
R602 1 Dummy 2 R0603 0_J
18 USB3_TX0_N
18 USB3_TX0_P
C0402 C442 1 2 0.1UF/10V,X5R SSTX1+_L
C0402 C443 1 2 0.1UF/10V,X5R SSTX1-_L
SSTX1-
SSTX1+
CHK7 _4p_choke
R599 1 Dummy 2 R0603 0_J
USB30_PWR
SBD0N
SBD1N
U55
AZC099-04S
SOT23_6
SBD0P
SBD1P
U59
Line-1
NC1
GND
Line-3
NC2
NC4
Line-2
NC3
Line-4
ESDA6V8UD
dfn2510p10e
R604 1 Dummy 2 R0603 0_J
18 USB3_RX1_N
18 USB3_RX1_P
SSRX2-
SSRX2+
CHK8 _4p_choke
R603 1 Dummy 2 R0603 0_J
R439 1 0_J 2 R0603
18 USB_PN1
18 USB_PP1
SBD1N
SBD1P
CHK12 _4p_choke
R441 1 0_J 2 R0603
USB30_PWR
C734
C0402
330PF/50V,X7R
USB2
UEA111JC-C14U6-7H
R607 1 Dummy 2 R0603 0_J
18 USB3_TX1_N
18 USB3_TX1_P
C0402 C444 1 2 0.1UF/10V,X5R SSTX2+_L
C0402 C445 1 2 0.1UF/10V,X5R SSTX2-_L
SSTX2-
SSTX2+
CHK9 _4p_choke
R605 1 Dummy 2 R0603 0_J
U60
ESDA6V8UD
dfn2510p10e
+5VSB
USB30_PWR
U16
GND
IN_1
IN_2
EN(EN#)
OUT_3
OUT_2
OUT_1
OC#
uP7534BRA8-15
MSOP8_0D65_2D54
USB30_OCJ 18
PPON1
C437
C0402
0.1UF/10V,X5R
R840
NC_0_J
R0402
NC
16,33,34,35,40,44 PM_SLP_S4#
R820 0_J
R0402
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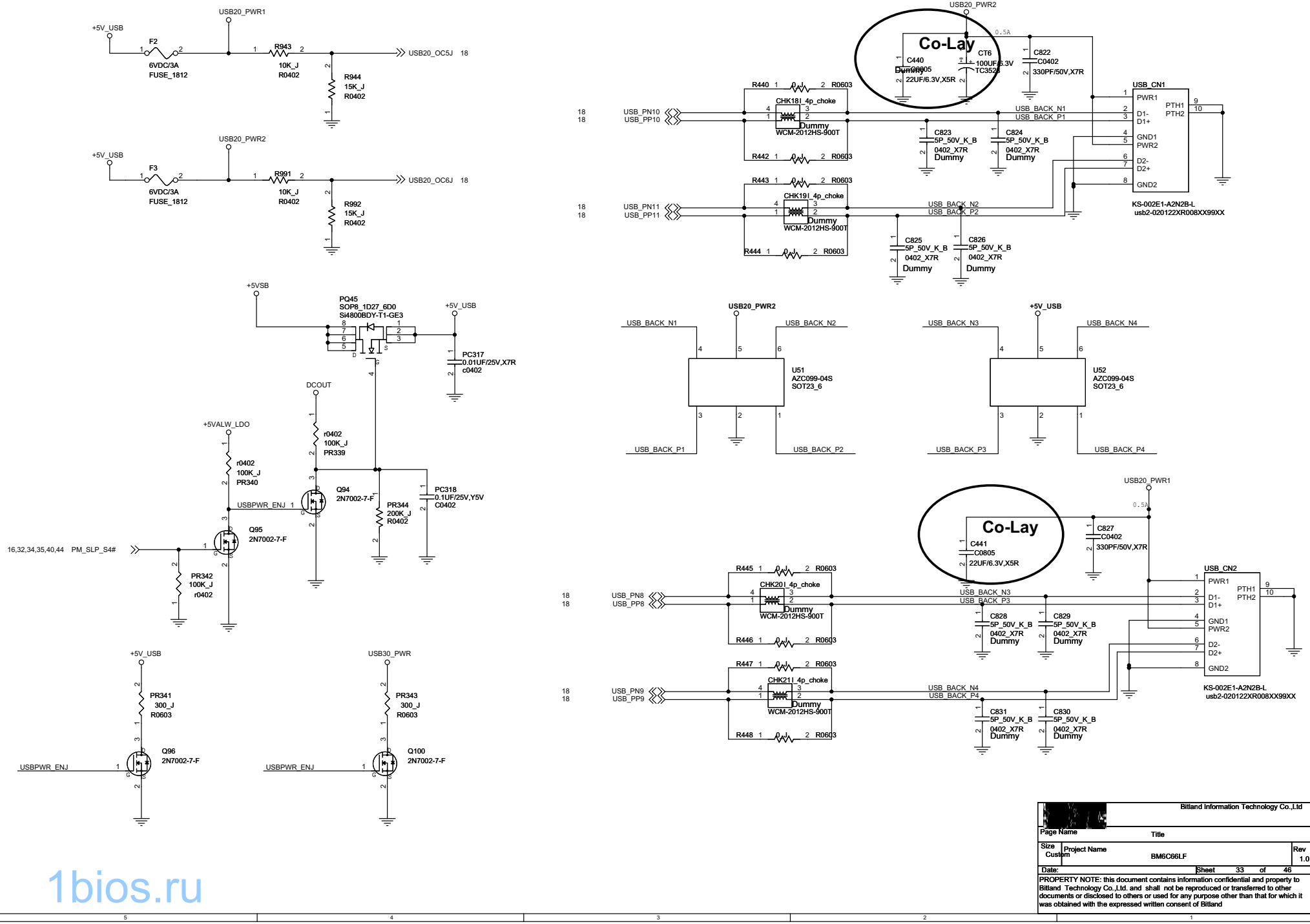
USB20_PWR1
+5V_USB
F2
6VDC/3A
FUSE_1812
R943
10K_J
R0402
R944
15K_J
R0402
USB20_OC5J 18
USB20_PWR2
+5V_USB
F3
6VDC/3A
FUSE_1812
R991
10K_J
R0402
R992
15K_J
R0402
USB20_OC6J 18
+5VSB
PQ45
SOP8_1D27_6D0
Si4800BDY-T1-GE3
+5V_USB
PC317
0.01UF/25V,X7R
c0402
DCOUT
+5VALW_LDO
r0402
100K_J
PR340
r0402
100K_J
PR339
USBPWR_ENJ 1
Q94
2N7002-7-F
PR344
200K_J
R0402
PC318
0.1UF/25V,Y5V
C0402
Q95
2N7002-7-F
16,32,34,35,40,44 PM_SLP_S4#
PR342
100K_J
r0402
+5V_USB
PR341
300_J
R0603
Q96
2N7002-7-F
USBPWR_ENJ 1
USB30_PWR
PR343
300_J
R0603
Q100
2N7002-7-F
USBPWR_ENJ 1
USB20_PWR2
Co-Lay
0.5A
C440
C0805
Dummy
22UF/6.3V,X5R
CT6
100UF/6.3V
TC3528
C822
C0402
330PF/50V,X7R
R440 1 0 J 2 R0603
CHK18I 4p_choke
Dummy
WCM-2012HS-900T
R442 1 0 J 2 R0603
R443 1 0 J 2 R0603
CHK19I 4p_choke
Dummy
WCM-2012HS-900T
R444 1 0 J 2 R0603
18 USB_PN10
18 USB_PP10
18 USB_PN11
18 USB_PP11
USB_BACK_N1
USB_BACK_P1
USB_BACK_N2
USB_BACK_P2
C823
5P_50V_K_B
0402_X7R
Dummy
C824
5P_50V_K_B
0402_X7R
Dummy
C825
5P_50V_K_B
0402_X7R
Dummy
C826
5P_50V_K_B
0402_X7R
Dummy
USB_CN1
PWR1
D1-
D1+
GND1
PWR2
D2-
D2+
GND2
PTH1
PTH2
KS-002E1-A2N2B-L
usb2-020122XR008XX99XX
USB20_PWR2
USB_BACK_N1
USB_BACK_N2
U51
AZC099-04S
SOT23_6
USB_BACK_P1
USB_BACK_P2
+5V_USB
USB_BACK_N3
USB_BACK_N4
U52
AZC099-04S
SOT23_6
USB_BACK_P3
USB_BACK_P4
USB20_PWR1
Co-Lay
0.5A
C441
C0805
22UF/6.3V,X5R
C827
C0402
330PF/50V,X7R
R445 1 0 J 2 R0603
CHK20I 4p_choke
Dummy
WCM-2012HS-900T
R446 1 0 J 2 R0603
R447 1 0 J 2 R0603
CHK21I 4p_choke
Dummy
WCM-2012HS-900T
R448 1 0 J 2 R0603
18 USB_PN8
18 USB_PP8
18 USB_PN9
18 USB_PP9
USB_BACK_N3
USB_BACK_P3
USB_BACK_N4
USB_BACK_P4
C828
5P_50V_K_B
0402_X7R
Dummy
C829
5P_50V_K_B
0402_X7R
Dummy
C831
5P_50V_K_B
0402_X7R
Dummy
C830
5P_50V_K_B
0402_X7R
Dummy
USB_CN2
PWR1
D1-
D1+
GND1
PWR2
D2-
D2+
GND2
PTH1
PTH2
KS-002E1-A2N2B-L
usb2-020122XR008XX99XX
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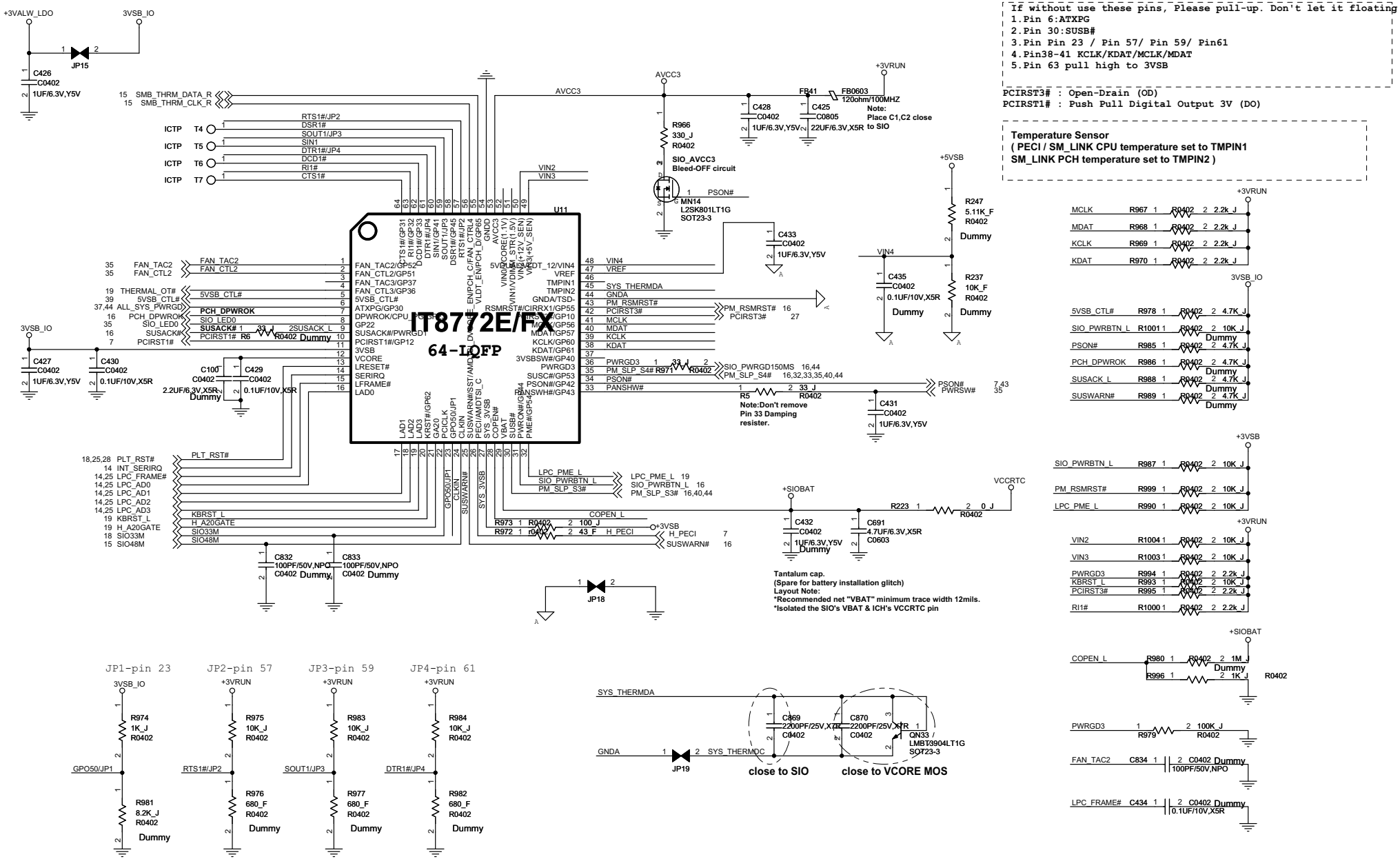

Power-On Strapping

	Symbol	Value	Description
JP1 Pin-23	DSW_EUP_SEL	1 *	EUP(default)
		0	DSW
JP2 Pin-57	WDT_EN	1 *	Disable WDT to reset PWROK(default)
		0	Enable WDT to reset PWROK
JP3 Pin-59	FAN_CTL_SEL	1 *	EC Index 6Bh/73h default = 80h
		0	EC Index 6Bh/73h default = 00h
JP4 Pin-61	K8PWR_EN	1 *	Disable K8 Power Sequence(default)
		0	Enable K8 Power Sequence

Note:
If 75232 is connected, please use 680 ohm to be the pull down resistor value. Since powered by 12V, 75232 has a very strong internal pull-up. It is hard to be pulled low. (Please see specification for detail of power on strapping setting)

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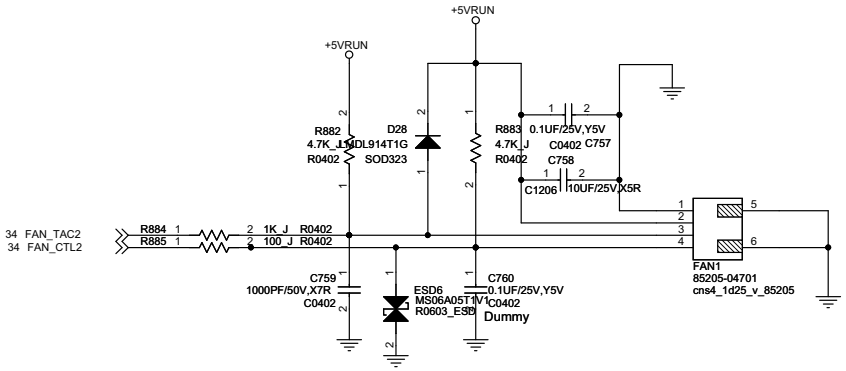
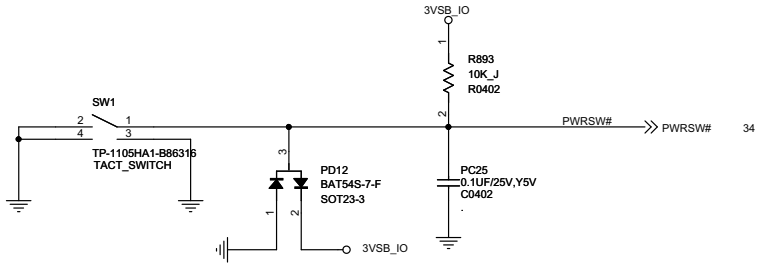
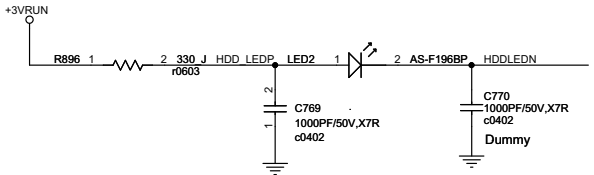
SYSTEM FAN

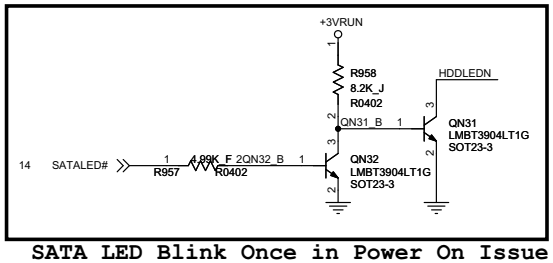


Power SW.



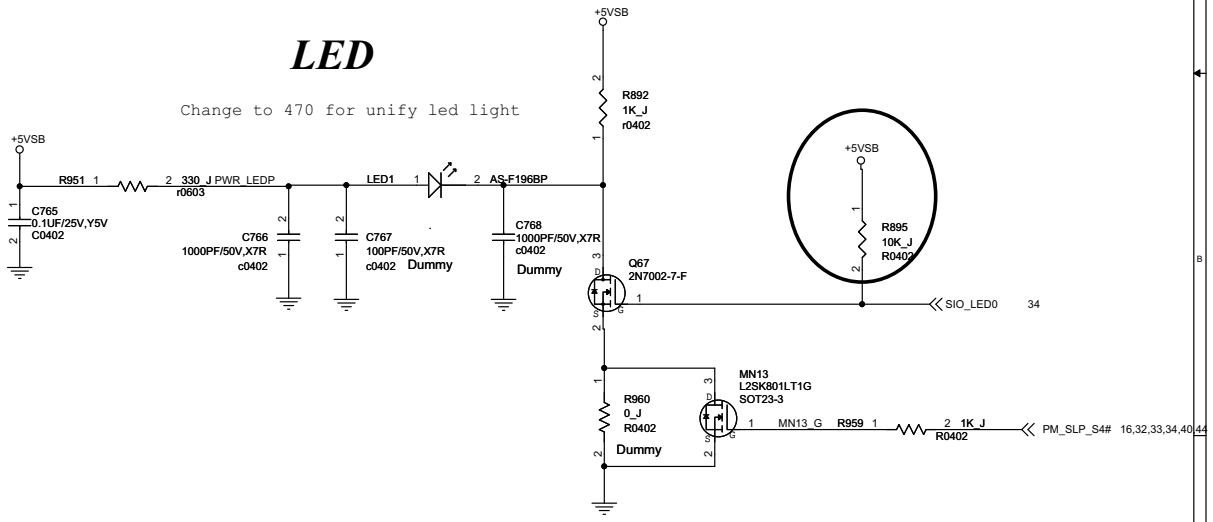
LED





SATA LED Blink Once in Power On Issue

Change to 470 for unify led light



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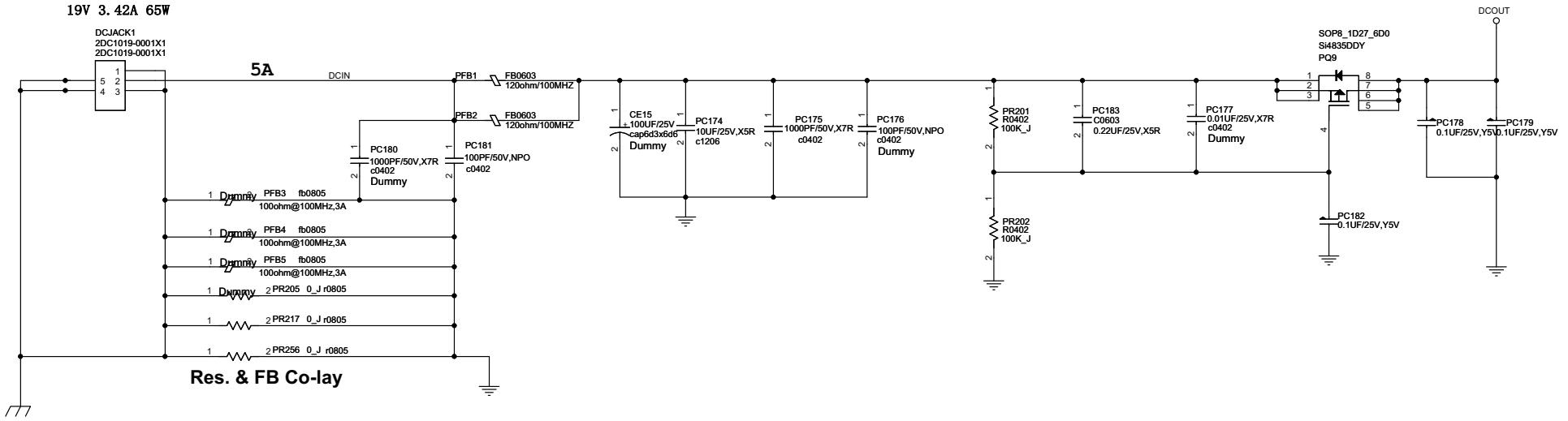

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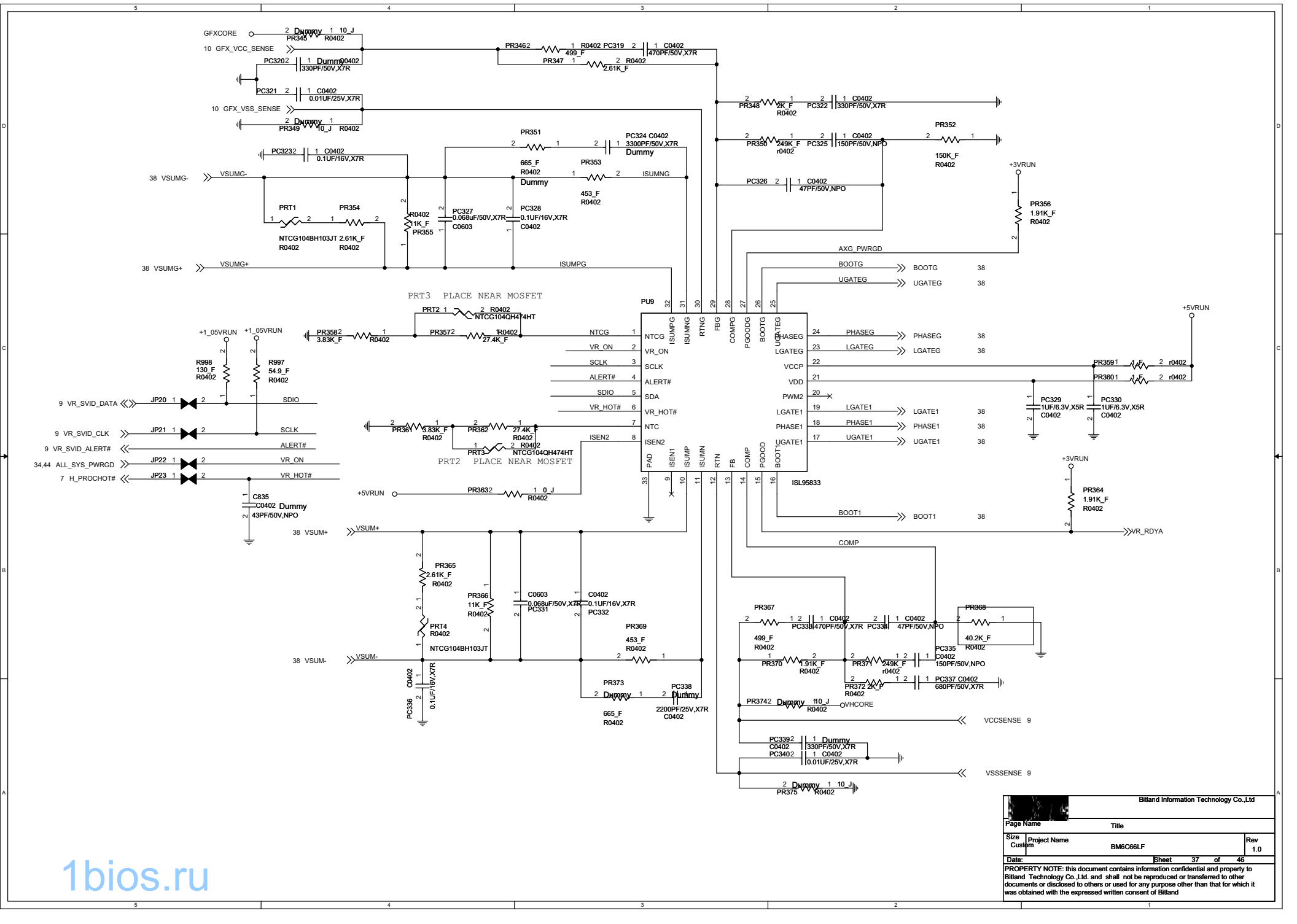
GFXCORE
10 GFX_VCC_SENSE
10 GFX_VSS_SENSE
38 VSUMG-
38 VSUMG+
PRT1
NTCG104BH103JT 2.61K_F
PRT3 PLACE NEAR MOSFET
PRT2 PLACE NEAR MOSFET
NTCG104QH474HT
PU9
ISL95833
+1_05VRUN
+5VRUN
+3VRUN
9 VR_SVID_DATA
9 VR_SVID_CLK
9 VR_SVID_ALERT#
34,44 ALL_SYS_PWRGD
7 H_PROCHOT#
38 VSUM+
38 VSUM-
AXG_PWRGD
VR_RDYA
VCCSENSE 9
VSSSENSE 9
VHCORE
Dummy
NTCG104BH103JT
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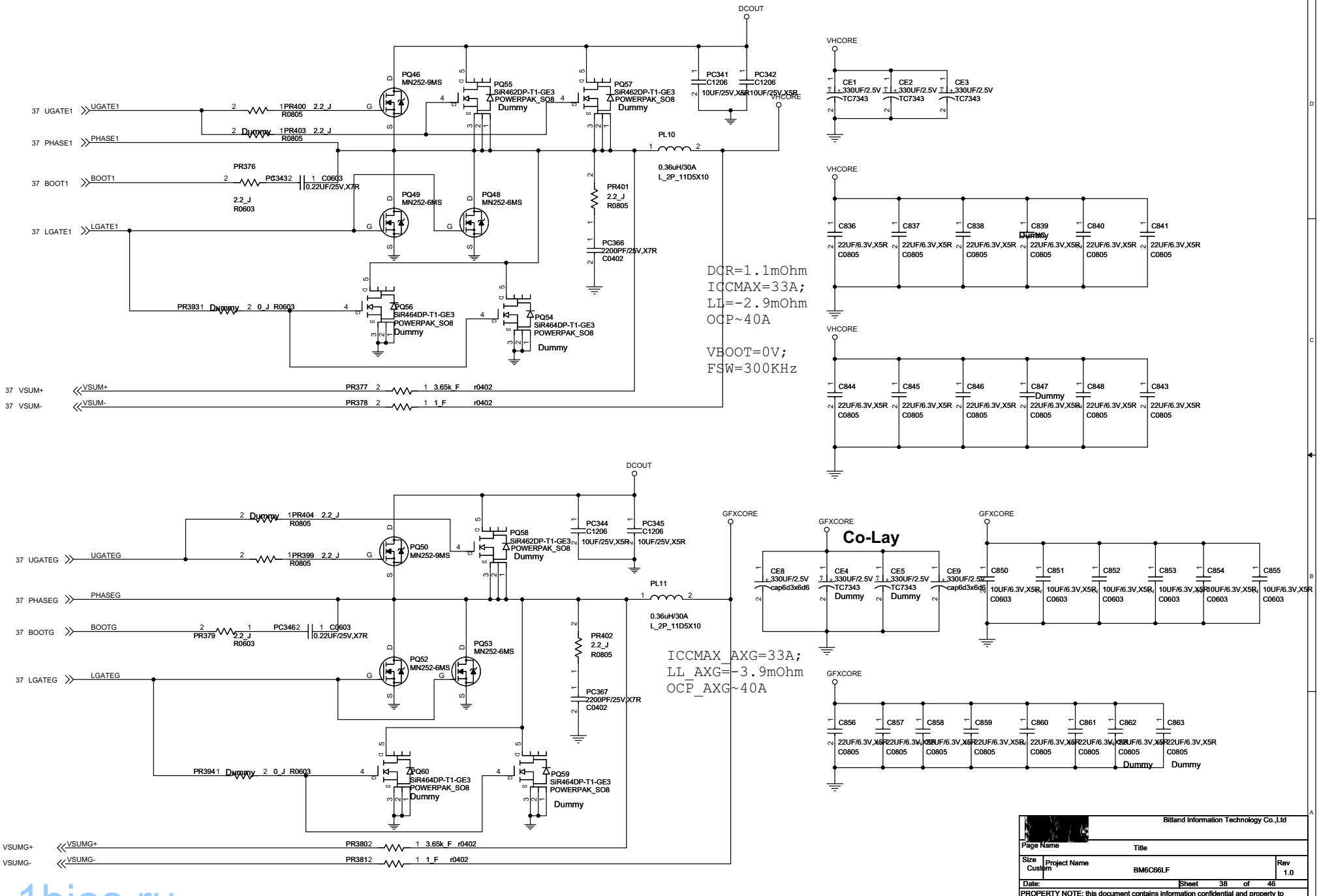
DCOUT
PQ46 MN252-9MS
PQ55 SiR462DP-T1-GE3 POWERPAK_SO8 Dummy
PQ57 SiR462DP-T1-GE3 POWERPAK_SO8 Dummy
PC341 C1206 10UF/25V,X5R
PC342 C1206 10UF/25V,X5R
VHCORE
37 UGATE1
UGATE1
PR400 2.2_J R0805
Dummy PR403 2.2_J R0805
37 PHASE1
PHASE1
PL10
0.36uH/30A
L_2P_11D5X10
PR376
37 BOOT1
BOOT1
PC343 C0603 0.22UF/25V,X7R
2.2_J R0603
PQ49 MN252-6MS
PQ48 MN252-6MS
37 LGATE1
LGATE1
PR401 2.2_J R0805
PC366 2200PF/25V,X7R C0402
PR393 Dummy 0_J R0603
PQ56 SiR464DP-T1-GE3 POWERPAK_SO8 Dummy
PQ54 SiR464DP-T1-GE3 POWERPAK_SO8 Dummy
37 VSUM+
VSUM+
PR377 3.65k_F r0402
37 VSUM-
VSUM-
PR378 1_F r0402
DCR=1.1mOhm
ICCMAX=33A;
LL=-2.9mOhm
OCP~40A
VBOOT=0V;
FSW=300KHz
CE1 330UF/2.5V TC7343
CE2 330UF/2.5V TC7343
CE3 330UF/2.5V TC7343
C836 C837 C838 C839 Dummy C840 C841
C844 C845 C846 C847 Dummy C848 C843
22UF/6.3V,X5R C0805
DCOUT
Dummy PR404 2.2_J R0805
PQ58 SiR462DP-T1-GE3 POWERPAK_SO8 Dummy
PC344 C1206 10UF/25V,X5R
PC345 C1206 10UF/25V,X5R
GFXCORE
37 UGATEG
UGATEG
PR399 2.2_J R0805
PQ50 MN252-9MS
37 PHASEG
PHASEG
PL11
0.36uH/30A
L_2P_11D5X10
37 BOOTG
BOOTG
PR379 2.2_J R0603
PC346 C0603 0.22UF/25V,X7R
PQ53 MN252-6MS
PQ52 MN252-6MS
37 LGATEG
LGATEG
PR402 2.2_J R0805
PC367 2200PF/25V,X7R C0402
PR394 Dummy 0_J R0603
PQ60 SiR464DP-T1-GE3 POWERPAK_SO8 Dummy
PQ59 SiR464DP-T1-GE3 POWERPAK_SO8 Dummy
37 VSUMG+
VSUMG+
PR380 3.65k_F r0402
37 VSUMG-
VSUMG-
PR381 1_F r0402
ICCMAX_AXG=33A;
LL_AXG=-3.9mOhm
OCP_AXG~40A
Co-Lay
CE8 330UF/2.5V cap6d3x6d6
CE4 330UF/2.5V TC7343 Dummy
CE5 330UF/2.5V TC7343 Dummy
CE9 330UF/2.5V cap6d3x6d6
C850 C851 C852 C853 C854 C855
10UF/6.3V,X5R C0603
C856 C857 C858 C859 C860 C861 C862 C863
22UF/6.3V,X5R C0805
Dummy
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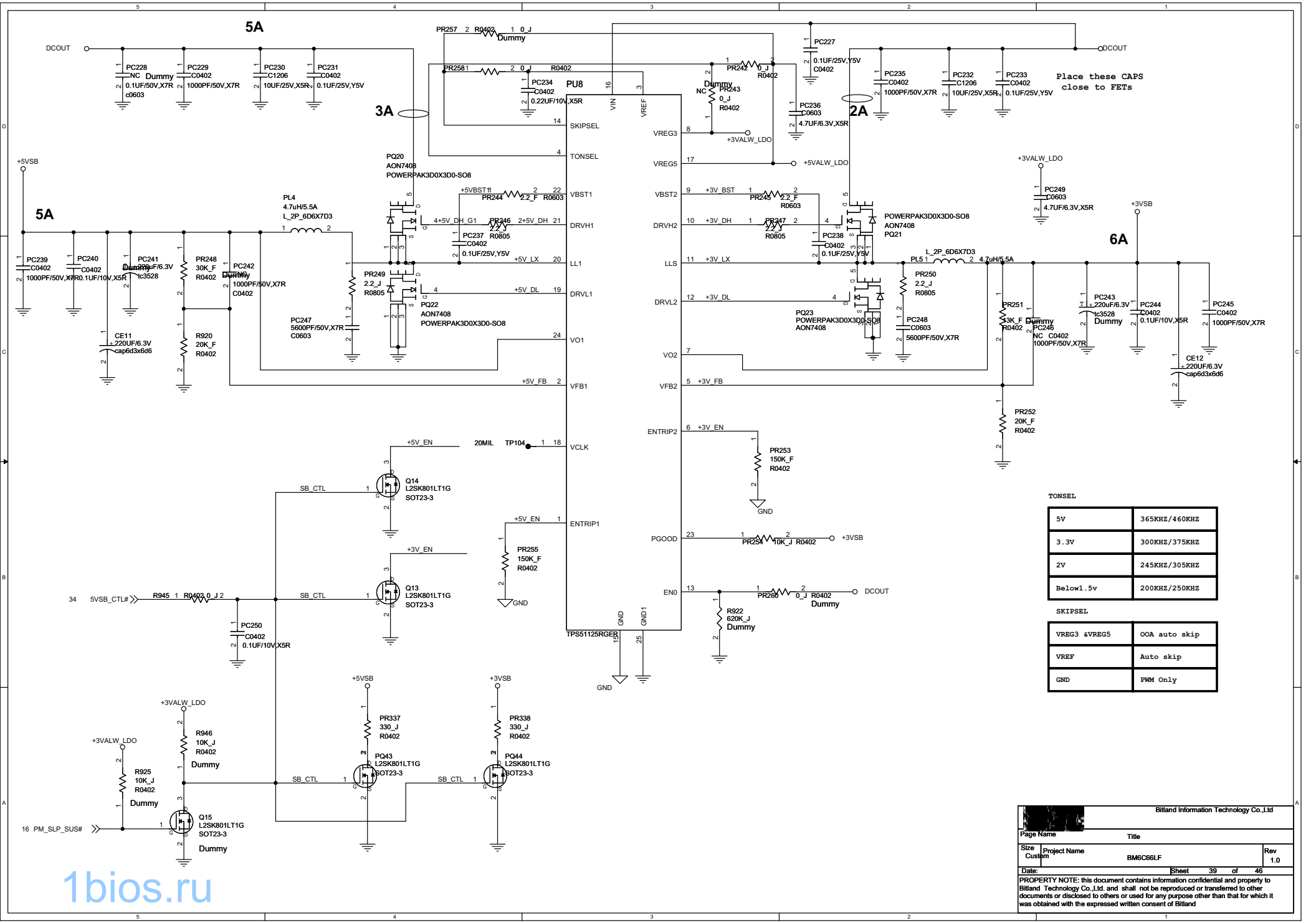
5A
3A
2A
6A
PU8
TPS51125RGER
Place these CAPS close to FETs
TONSEL
5V 365KHZ/460KHZ
3.3V 300KHZ/375KHZ
2V 245KHZ/305KHZ
Below1.5v 200KHZ/250KHZ
SKIPSEL
VREG3 &VREG5 OOA auto skip
VREF Auto skip
GND PWM Only
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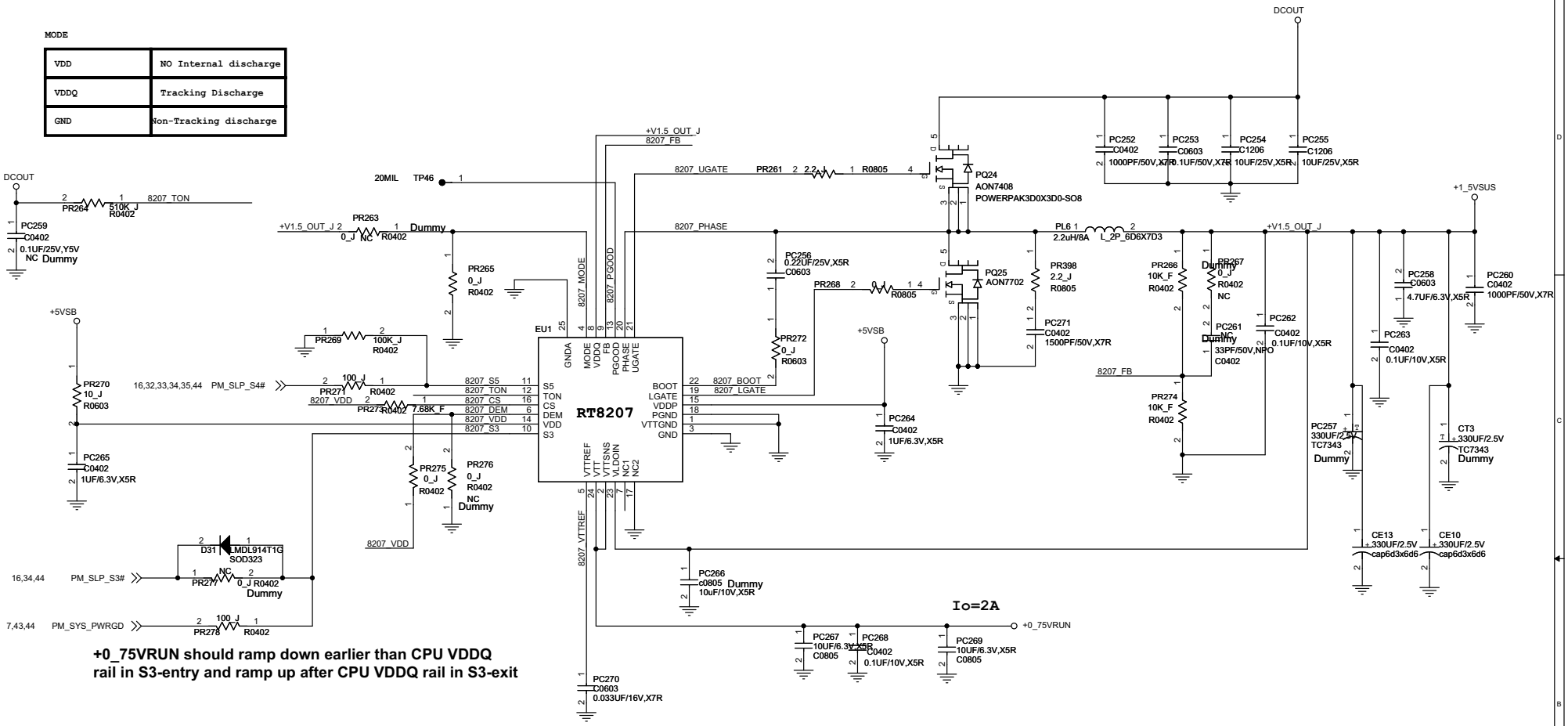
MODE

VDD	NO Internal discharge
VDDQ	Tracking Discharge
GND	Non-Tracking discharge



+0_75VRUN should ramp down earlier than CPU VDDQ rail in S3-entry and ramp up after CPU VDDQ rail in S3-exit

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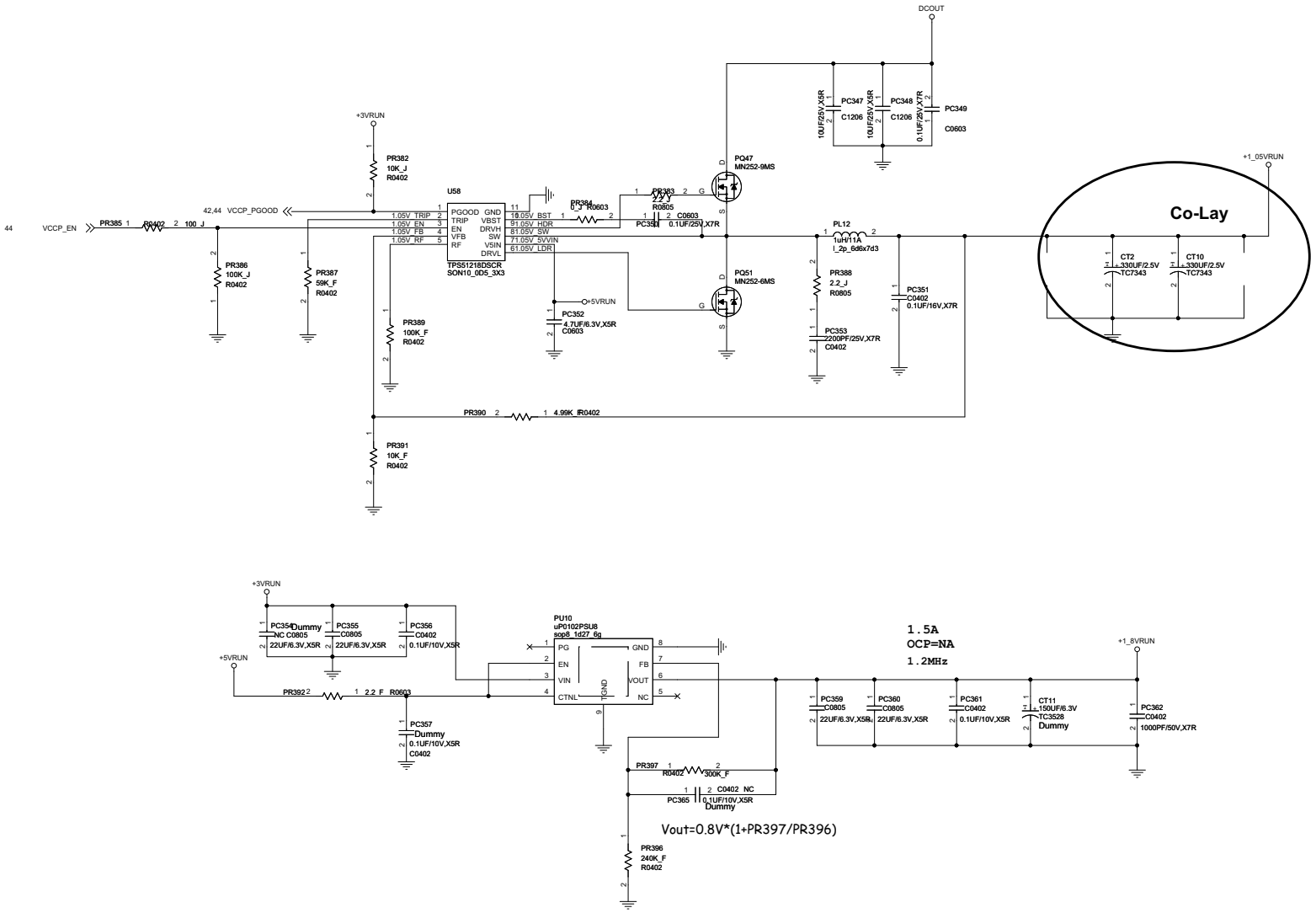

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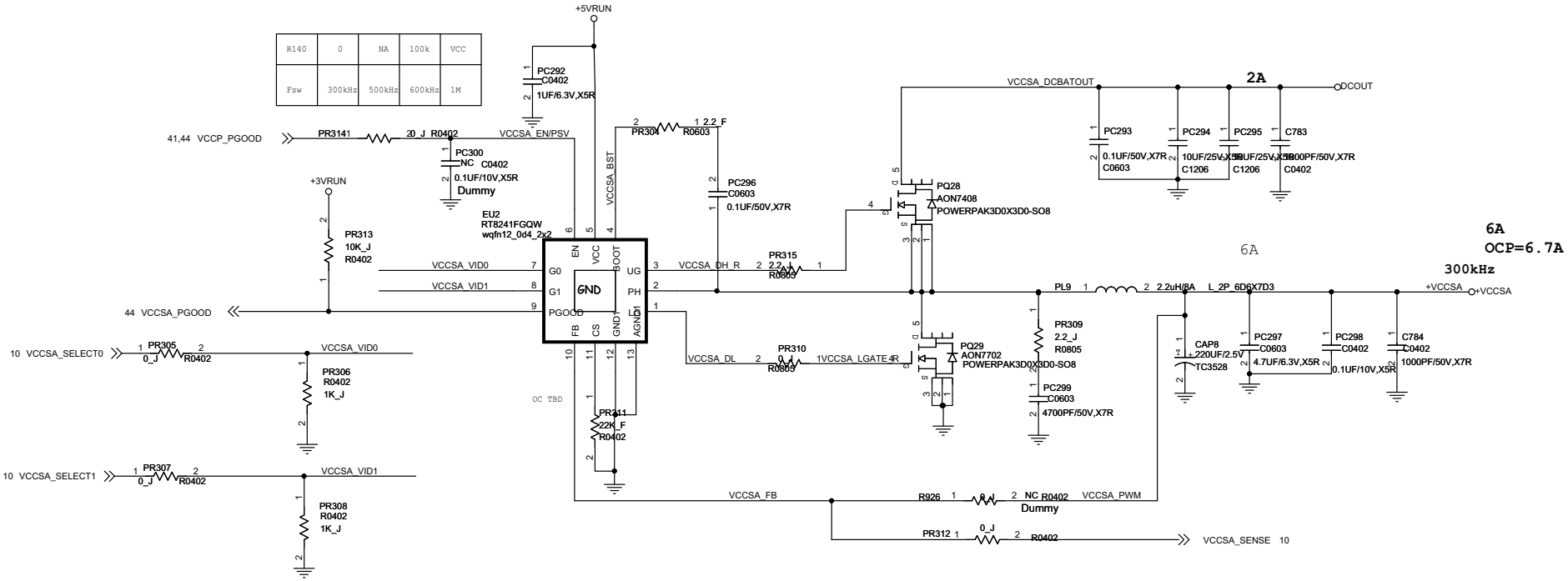

		VID1	VID0
Vout1	0.675V	1	1
Vout2	0.725V	0	1
Vout3	0.8V	1	0
Vout4	0.9V	0	0

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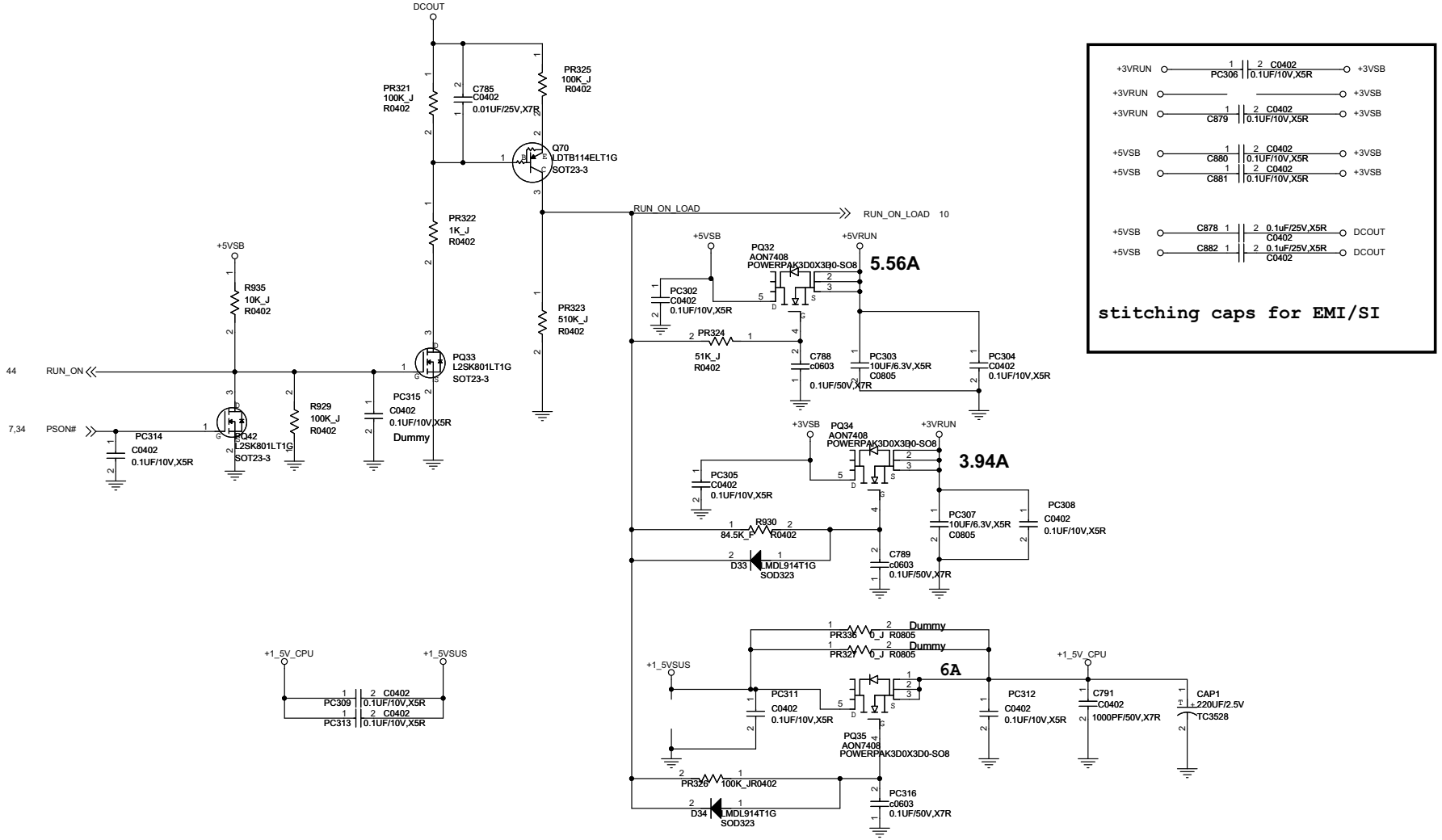

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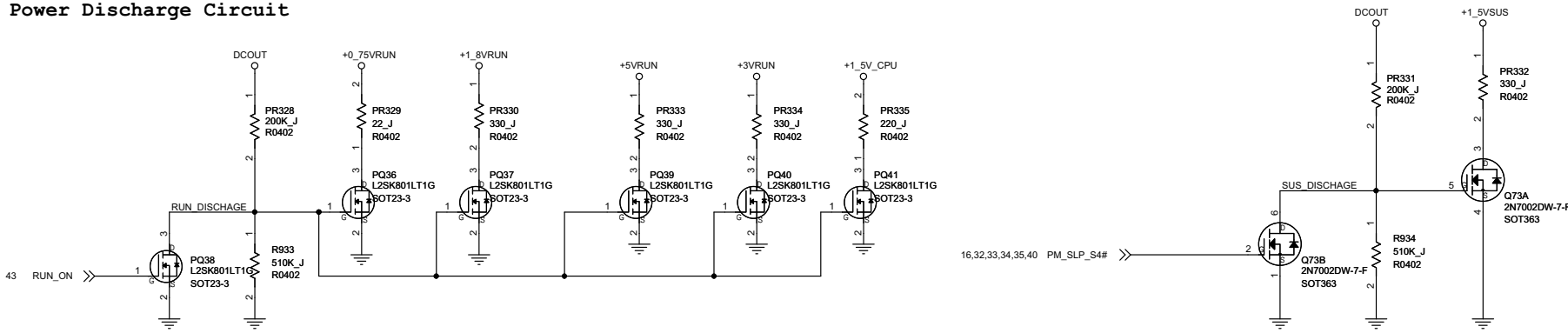
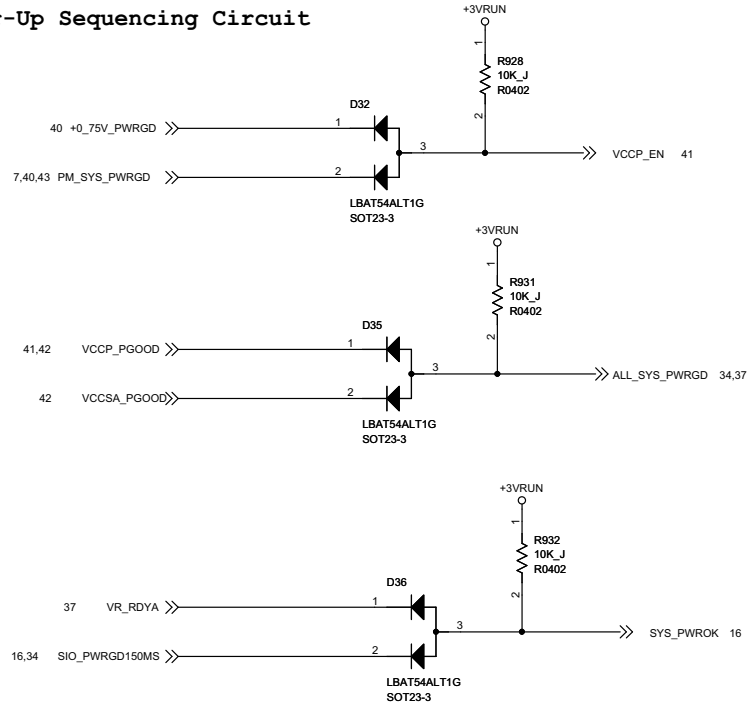
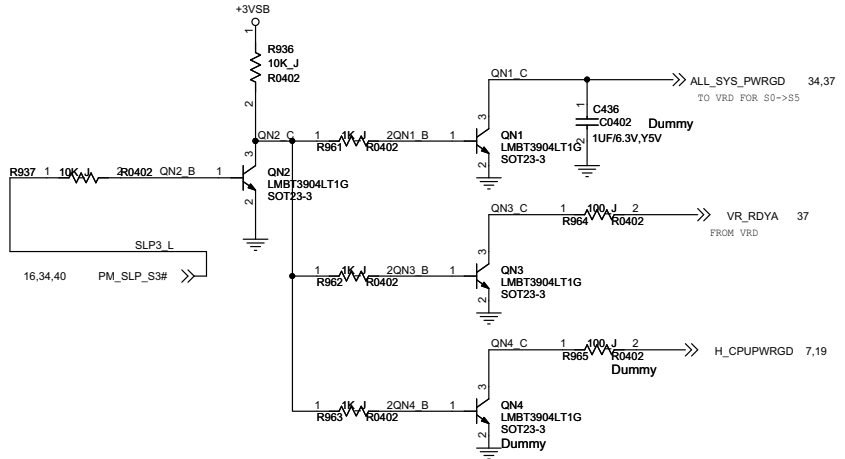
Power Discharge Circuit



Power-Up Sequencing Circuit



Power Down Sequencing Circuit



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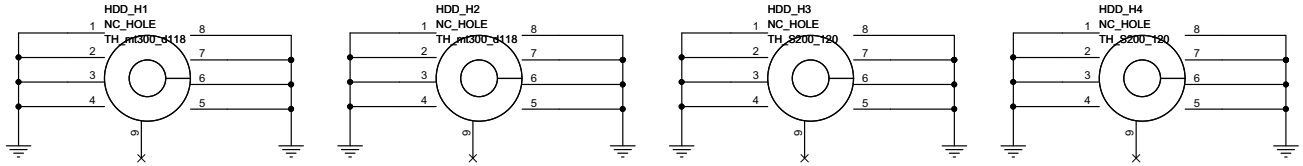

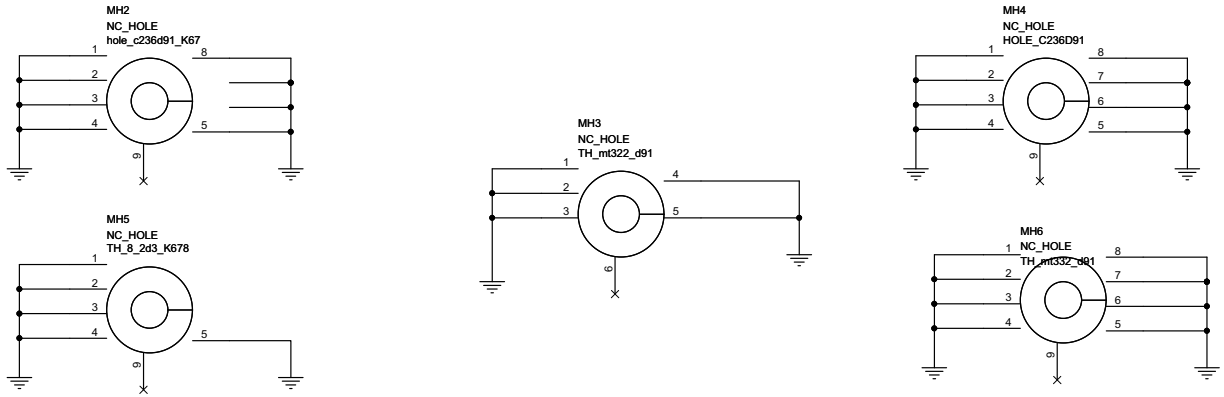

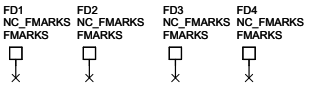

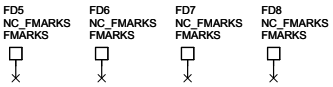

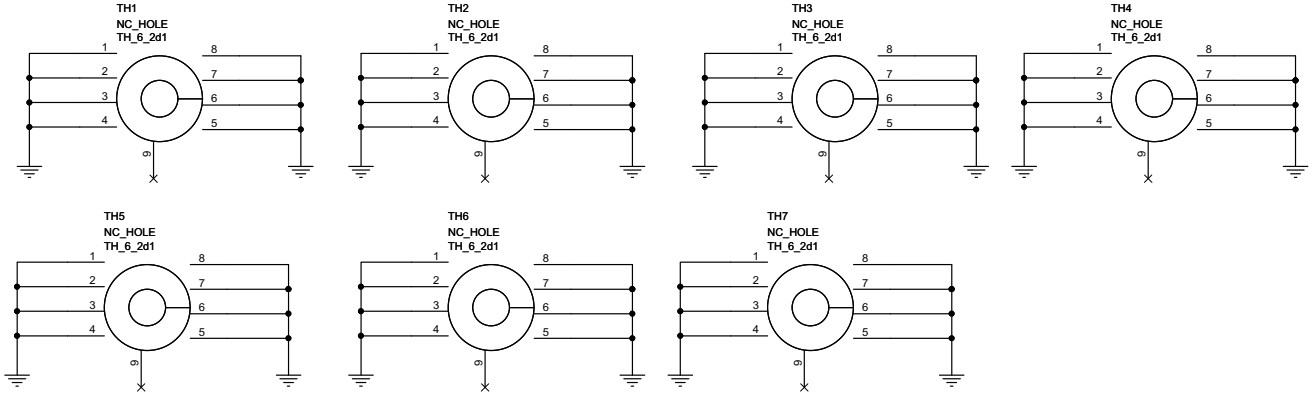

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REVISION HISTORY:

Rev	Date	Notes
V0.1	12/03/20	
V0.2	XX/XX/XX	

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